MIO

SERVICE MANUAL

VERSION 2.0

METALGUY66/WARERAT

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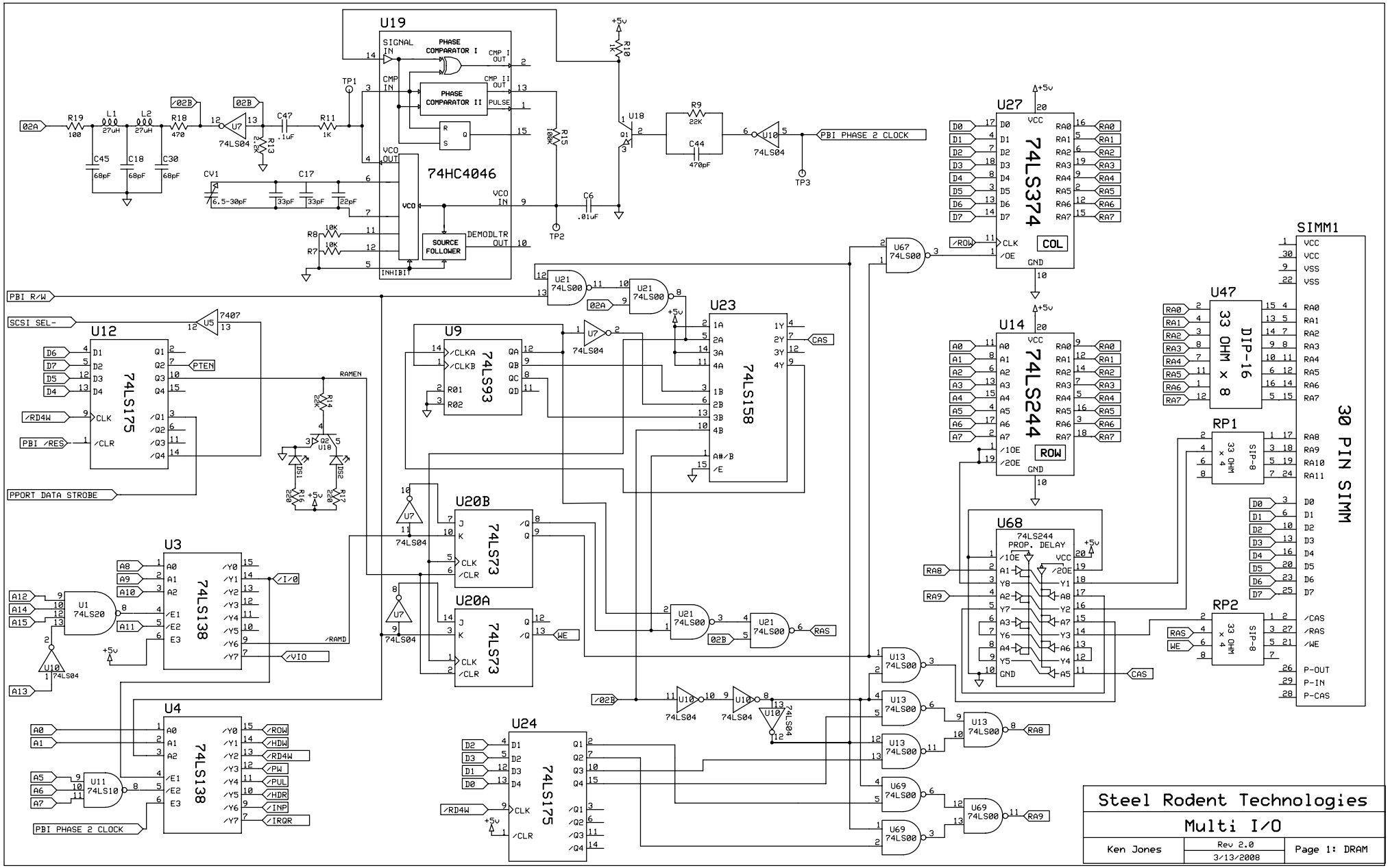
U19
74HC4046
SIGNAL IN
PHASE COMPARATOR I
PHASE COMPARATOR II
CMP I OUT
CMP II OUT
PULSE
CMP IN
VCO OUT
VCO IN
VCO
INHIBIT
SOURCE FOLLOWER
DEMODLTR OUT
74LS374
COL
74LS244
ROW
74LS175
74LS93
74LS158
74LS73
74LS138
74LS20
74LS10
74LS00
74LS04
74LS244
PROP. DELAY
DIP-16
33 OHM x 8
SIP-8
33 OHM x 4
SIMM1
30 PIN SIMM
PBI R/W
SCSI SEL-
PBI /RES
/RD4W
PTEN
RAMEN
PPORT DATA STROBE
PBI PHASE 2 CLOCK
/02A
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/I/O
/VIO
/RAMD
/ROW
/HDW
/RD4W
/PW
/PUL
/HDR
/INP
/IRQR
WE
RAS
CAS
/CAS
/RAS
/WE
P-OUT
P-IN
P-CAS
Steel Rodent Technologies
Multi I/O
Ken Jones
Rev 2.0
3/13/2008
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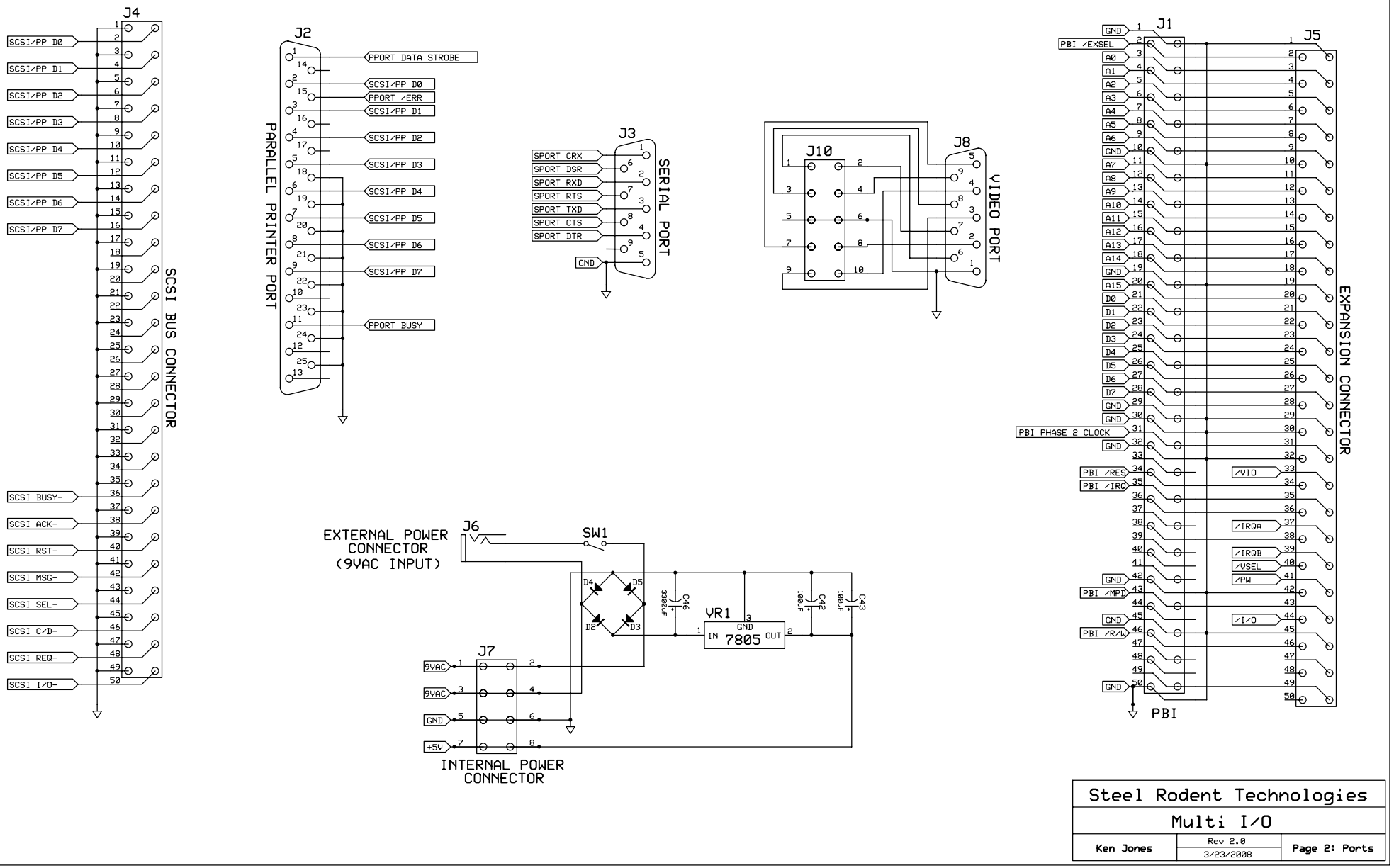
J4
SCSI BUS CONNECTOR
SCSI/PP D0
SCSI/PP D1
SCSI/PP D2
SCSI/PP D3
SCSI/PP D4
SCSI/PP D5
SCSI/PP D6
SCSI/PP D7
SCSI BUSY-
SCSI ACK-
SCSI RST-
SCSI MSG-
SCSI SEL-
SCSI C/D-
SCSI REQ-
SCSI I/O-
J2
PARALLEL PRINTER PORT
PPORT DATA STROBE
SCSI/PP D0
PPORT /ERR
SCSI/PP D1
SCSI/PP D2
SCSI/PP D3
SCSI/PP D4
SCSI/PP D5
SCSI/PP D6
SCSI/PP D7
PPORT BUSY
J3
SERIAL PORT
SPORT CRX
SPORT DSR
SPORT RXD
SPORT RTS
SPORT TXD
SPORT CTS
SPORT DTR
GND
J10
J8
VIDEO PORT
J1
J5
EXPANSION CONNECTOR
GND
PBI /EXSEL
A0
A1
A2
A3
A4
A5
A6
GND
A7
A8
A9
A10
A11
A12
A13
A14
GND
A15
D0
D1
D2
D3
D4
D5
D6
D7
GND
GND
PBI PHASE 2 CLOCK
GND
PBI /RES
PBI /IRQ
/VIO
/IRQA
/IRQB
/VSEL
/PW
GND
PBI /MPD
GND
PBI /R/W
/I/O
GND
PBI
EXTERNAL POWER CONNECTOR (9VAC INPUT)
J6
SW1
D4
D5
D2
D3
3300µF
C46
VR1
GND
IN
7805
OUT
100µF
C42
100µF
C43
J7
9VAC
9VAC
GND
+5V
INTERNAL POWER CONNECTOR
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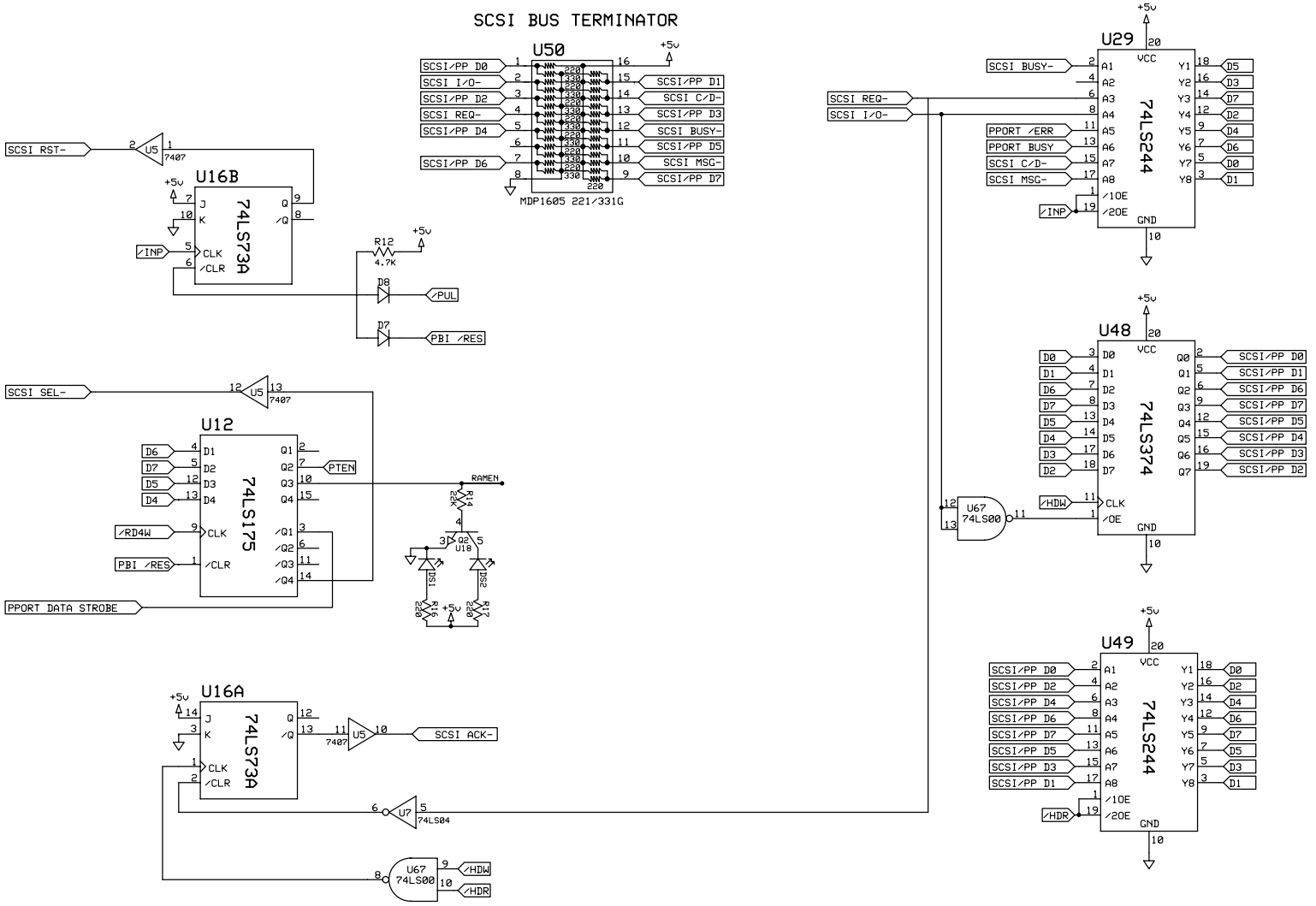

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Multi I/O		
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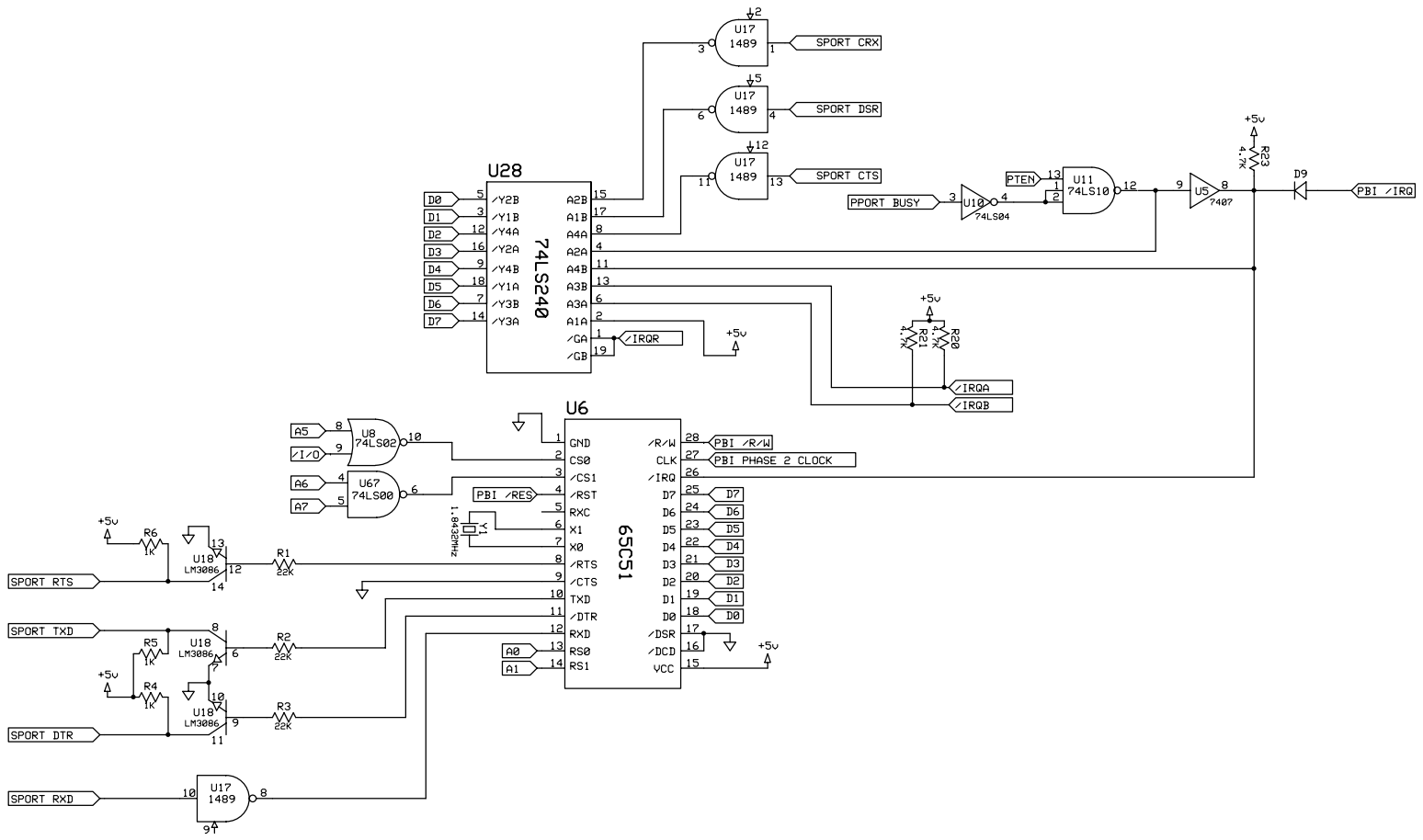

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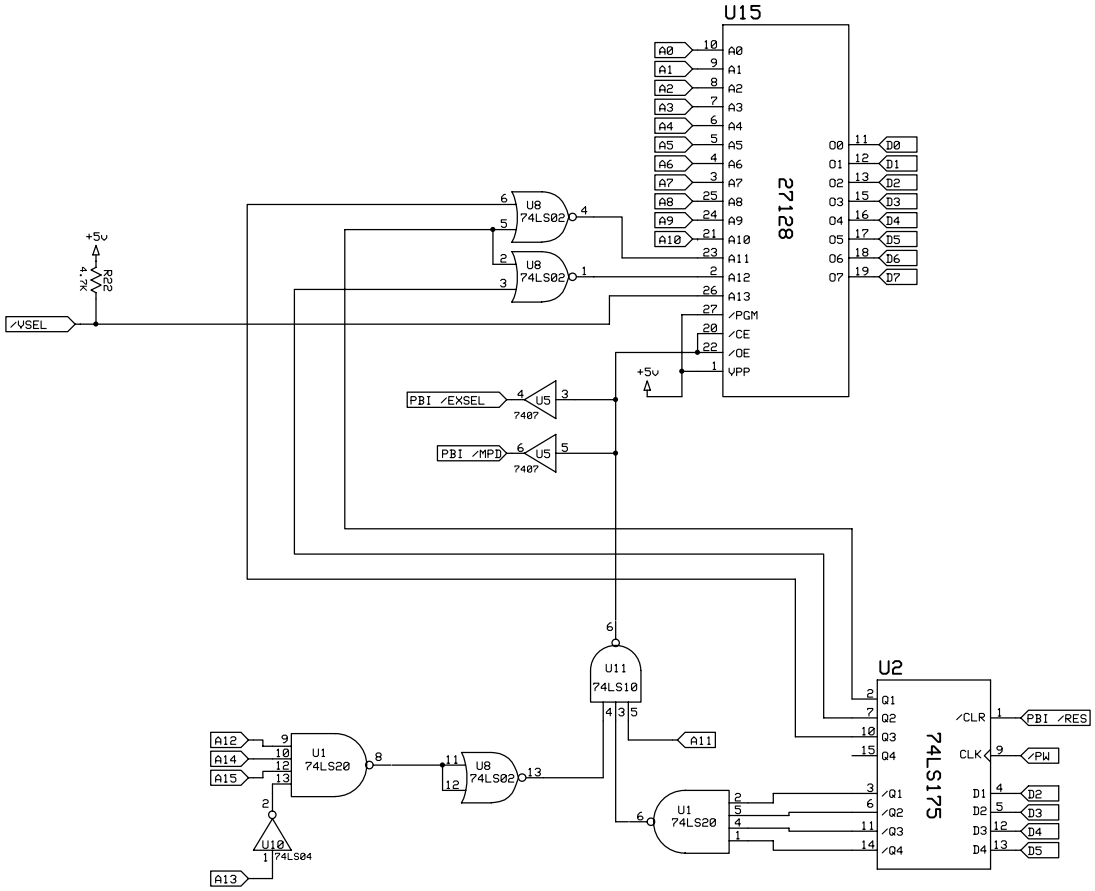
Multi I/O		
Ken Jones	Rev 2.0 3/27/2008	Page 4: Serial



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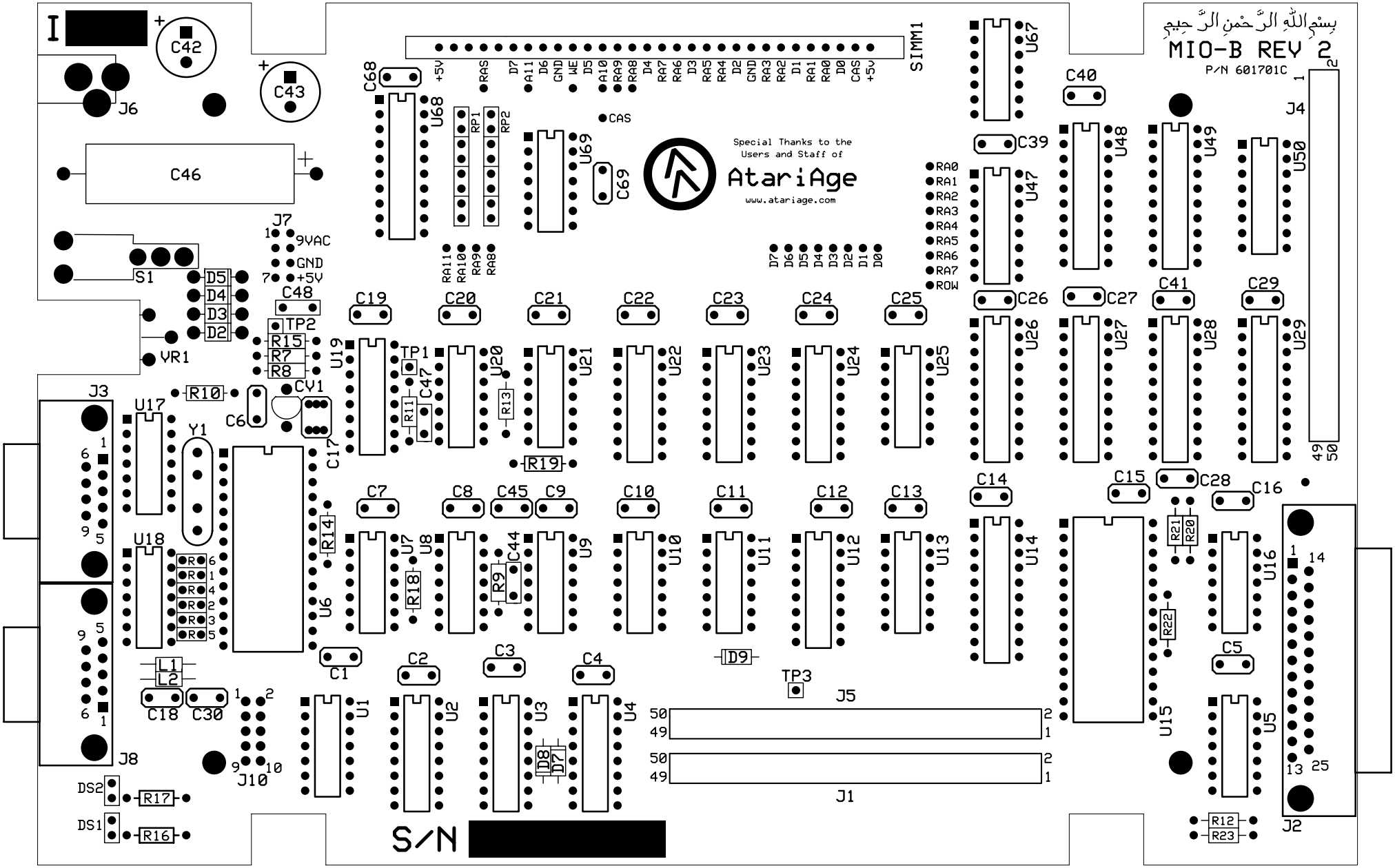
بِسْمِ اللهِ الرَّحْمنِ الرَّحِيمِ
MIO-B REV 2
P/N 601701C
SIMM1
Special Thanks to the
Users and Staff of
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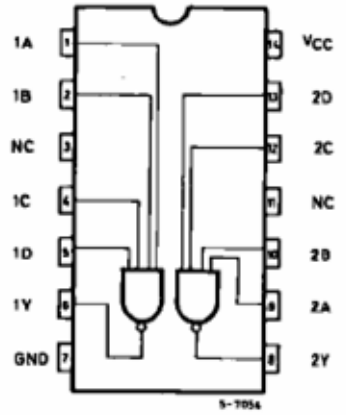
J1
J2
J3
J4
J5
J6
J7
J8
J10
S1
YR1
CY1
Y1
TP1
TP2
TP3
9VAC
GND
+5V
S/N

Description	Value	Qty per MIO	Layout number	Mouser number	Digikey number	cost
Transistor Array	LM3086N	1	U18	526-NTE912		$5.18
Quad Line Reciever	MC1489P	1	U17	511-MC1489P		$0.28
dual 4-input NAND gate	74HC20N	1	U1	511-M74HC20		$0.19
Hex Inverter	74LS04N	2	U7,U10		296-1629-5-ND	$0.29
12v Phase locked loop (obsolete- very early MIOs only)	MC14046	1	U19		MC14046BCPOS-ND	$0.52
5v Phase locked loop	MM74HC4046N	1	U19	512-MM74HC4046N		$0.45
Quad D-Type Flip Flop	74LS175	3	U2,U12,U24	595-SN74LS175N		$0.45
3 to 8 Line decoder/demultiplexer; Inverting	74HC138N	2	U3,U4		296-1575-5-ND	$0.27
Quad 2-input NOR gate	74LS02N	1	U8		296-1627-5-ND	$0.39
Dual J-K Flip Flop	HD74LS73P	2	U16,U20	526-NTE74LS73		$1.38
4-bit binary counter	74LS93	2	U9,U25		296-3750-5-ND	$0.94
quadruple 2-input positive NAND gate	HD74LS00P	4	U13,U21,U67,U69		296-1626-5-ND	$0.29
dual 1-of-4 Decoder/Demultiplexer	SN74LS139N	1	U22	595-SN74LS139AN		$0.38
quad 2-input multiplexer	74LS158	1	U23	526-NTE74LS158		$1.22
triple 3-input NAND gate	74HC10	1	U11	511-M74HC10		$0.20
Octal 3-state buffer/line-driver	SN74LS244N	5	U14,U26,U29,U49,U68		296-1653-5-ND	$0.45
Octal D-type Flip Flop, positive edge trigger, 3-state	74HCT374N	2	U27,U48		568-1543-5-ND	$0.30
Hex Buffer/Driver with open-collector high voltage Outputs	SN7407N	1	U5		296-1436-5-ND	$0.80
Octal 3-state buffer/line-driver	SN74LS240N	1	U28		296-1651-5-ND	$0.60
8 resistor network (isolated)	MDP1603-330G	1	U47	71-MDP1603-33		$0.52
16pin resistor network, dual-line terminated, pulse squaring	MDP1605 221/331G	1	U50	71-MDP1605131AGD04	4116R-3-221/331-ND	$1.03
27128 EPROM		1	U15			
6551 UART		1	U6			
DIP SOCKET, 14PIN		25		517-ICO-143-S8A-T		$0.08
DIP SOCKET, 16 PIN		10		517-ICO-163-S8A-T		$0.11
DIP SOCKET, 20 PIN		9		517-ICO-203-S8A-T		$0.11
DIP SOCKET, 28 PIN		2		517-ICO-286-S8A-T		$0.15
25x2 Pin Header, Right angle		1			A32706-25-ND	$1.74
25x2 Pin header		4			A32707-25-ND	$2.12
Female DB9 connector		1	J8	152-3409		$0.73
Male DB9 Connector		1	J3	152-3309		$0.77
Female DB25 connector		1	J2	152-3425		$1.19
Power connector		1	J6		CP-102AH-ND	$0.36
Power switch		1	S1	611-7101-061		$3.90
Red LED		1	DS2	606-4305H1		$0.21
Green LED		1	DS1	606-4305H5		$0.21
Oscillator	1.8432mhz	1	Y1	815-AB-1.8432-B2		$1.00
capacitor, ceramic,multilayer , .1uF	104/15z	35	c1-c5,c7-c16,c19-c29,c39-c41,c47,c68,c69		399-4209-ND	$0.05
capacitor, ceramic ,multilayer, 68pF	680/R5K	6	c18,c30,c45,CV1		399-4247-ND	$0.16
capacitor, ceramic,multilayer , .01uF	103/R5M	1	c6		399-4208-ND	$0.12
capacitor, mica, 22pF	220/J5	1	c17		399-4220-ND	$0.21
capacitor,ceramic,multilayer , 470pF	471k/5a	2	c44,c48		399-4242-ND	$0.13
capacitor, electrolytic	3300uf,16v	1	c46		4043PHBK-ND	$2.08
capacitor, electrolytic	220uf,25v	2	c42,c43		493-1319-ND	$0.27
resistor	1k,1/4w	8	r4-r8,r10,r11		1.0KQBK-ND	$0.01
resistor	100k,1/4w	1	r15		100KQBK-ND	$0.02
resistor	2.2k,1/4w	1	r13		2.2KQBK-ND	$0.02
resistor	220,1/4w	2	r16,r17		220QBK-ND	$0.02
resistor	22k,1/4w	5	r1-r3,r9,r14		22KQBK	$0.02
resistor	470,1/4w	1	r18		470QBK-ND	$0.02
resistor	100,1/4w	1	r19		100QBK-ND	$0.02
resistor	4.7k,1/4w	5	r12,r20-r23		3.7KQBK-ND	$0.02
signal diode	1N4/148/H	5	d1,d6,d7,d8,d9	78-1N4148		$0.02
rectifier diode	DT/1N4003	4	d2-d5			
voltage regulator	7805A	1	VR1	511-L7805ABP		$0.47
voltage regulator	428/340LA/15	1	VR2	512-MC78L15ACP		$0.26
Variable Capacitor (obsolete- replaced with two 68pF caps)		1	CV1	659-GKG30015		$0.21
Inductor, Ceramic	27uH, 10%	2	L1,L2		M8030-ND	$0.52
50 conductor Card-edge crimp connector			used to make MIO-ATARI cable		CCE50G-ND	$4.79

U1
74LS20 DUAL 4-INPUT NAND GATE

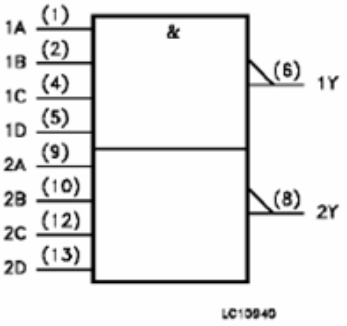
PIN CONNECTIONS (top view)



TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

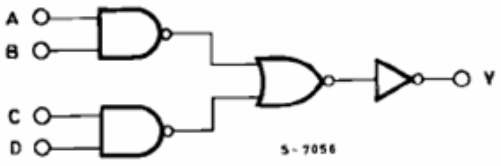
IEC LOGIC SYMBOL



PIN DESCRIPTION

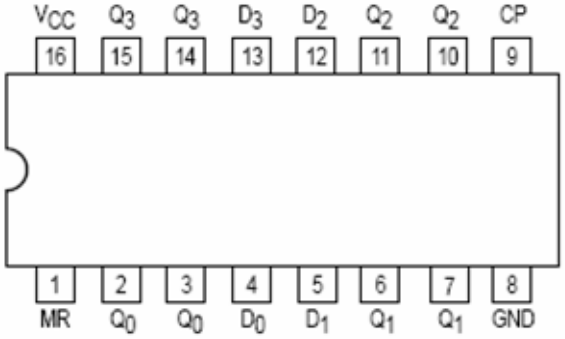
PIN No	SYMBOL	NAME AND FUNCTION
1, 9	1A to 2A	Data Inputs
2, 10	1B to 2B	Data Inputs
3, 11	N. C.	Not Connected
4, 12	1C, 2C	Data Inputs
5, 13	1D, 2D	Data Inputs
6, 8	1Y to 2Y	Data Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

SCHEMATIC CIRCUIT (Per Gate)



U2, U12, U24
74LS175 QUAD D FLIP-FLOP

CONNECTION DIAGRAM DIP (TOP VIEW)



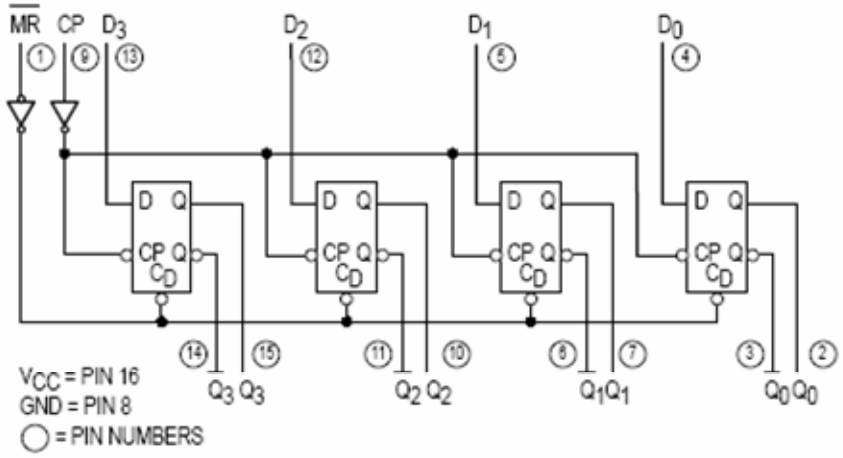
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

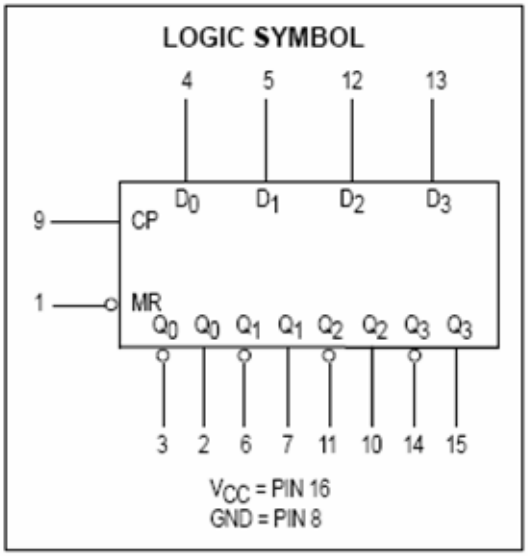
PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0-D_3	Data Inputs	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
MR	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{Q}_0-\overline{Q}_3$	True Outputs (Note b)	10 U.L.	5 (2.5) U.L.
Q_0-Q_3	Complemented Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM





FUNCTIONAL DESCRIPTION

The LS175 consists of four edge-triggered D flip-flops with individual D inputs and Q and Q outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW to HIGH Clock (CP) transition, causing individual Q and Q outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and Q outputs HIGH independent of Clock or Data inputs.

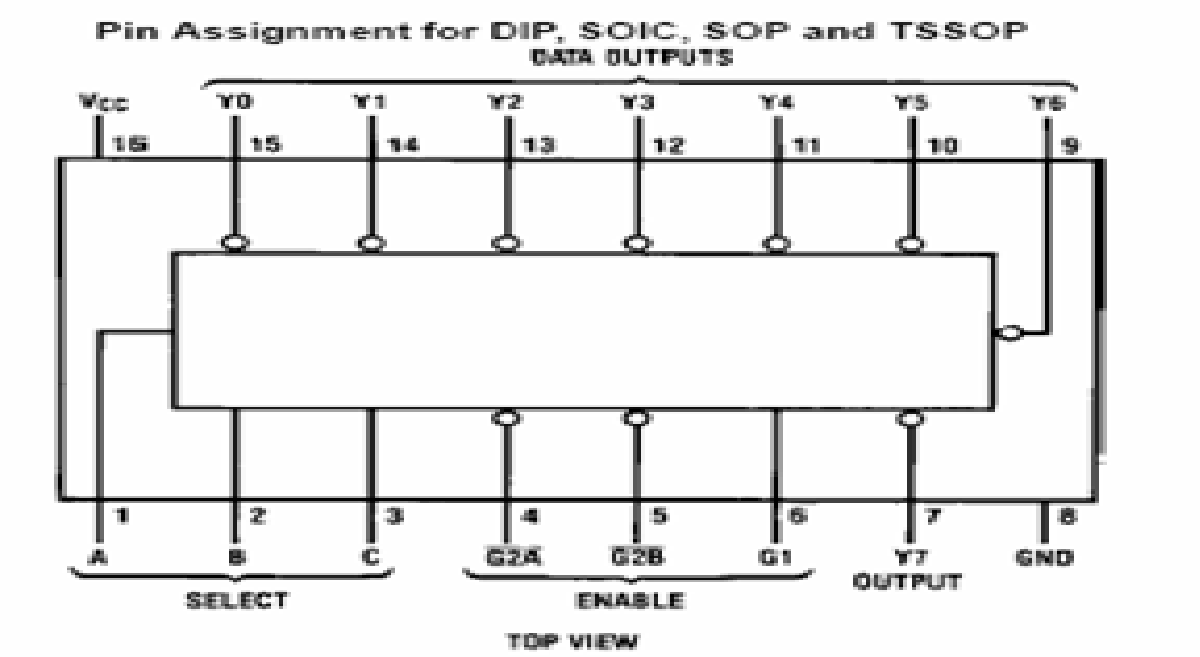
The LS175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n+1) Note 1	
D	Q	Q
L	L	H
H	H	L

Note 1: t = n + 1 indicates conditions after next clock.

U3, U4
74LS138 3-TO-8 LINE DECODER



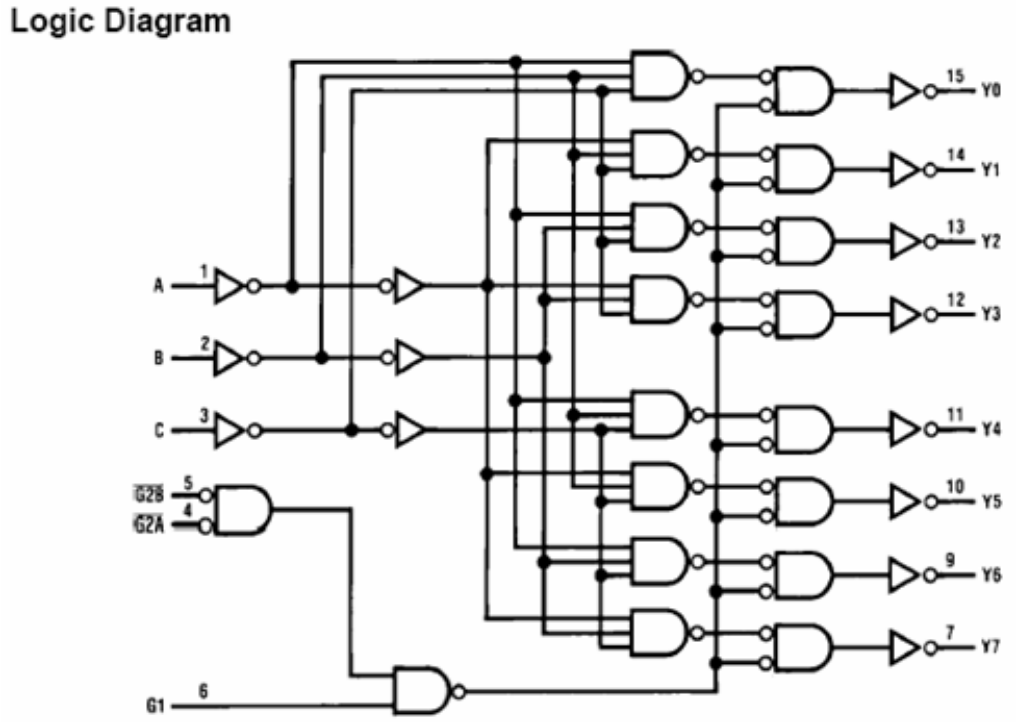
Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

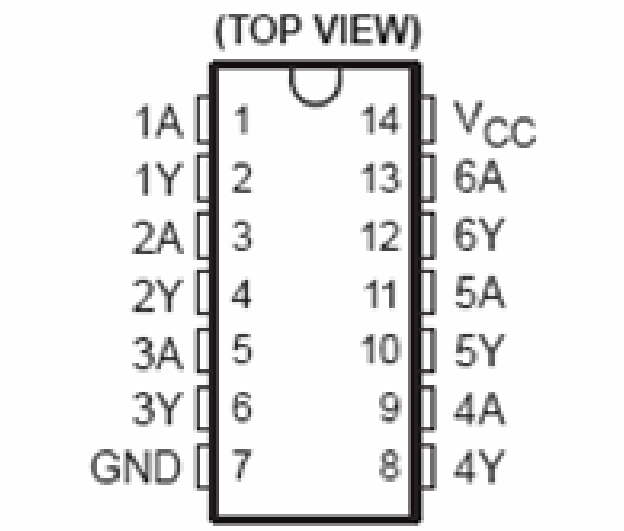
H = HIGH Level, L = LOW Level, X = don't care

Note 1: $\overline{G2}$ = G2A+G2B

Logic Diagram

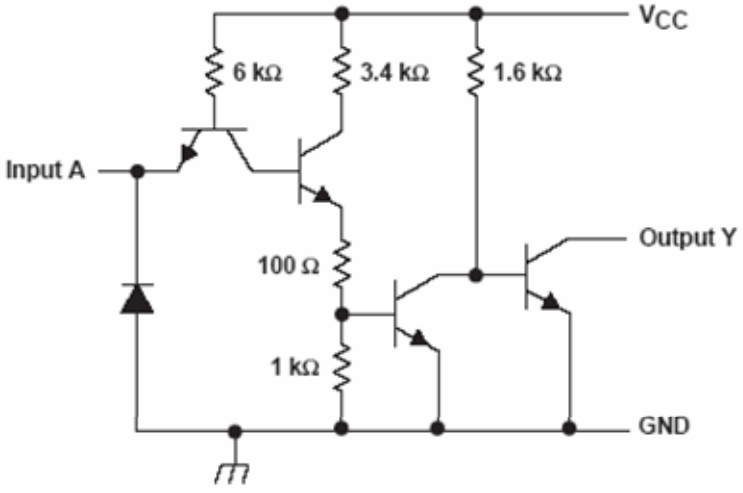


U5
7407 HEX BUFFER/DRIVER



logic diagram, each buffer/driver (positive logic)

schematic



U6
6551 ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

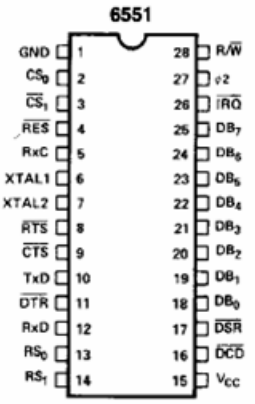
Features

- On-chip baud rate generator: 15 programmable baud rates derived from a standard 1.8432 MHz external crystal (50 to 19,200 baud).
- Programmable interrupt and status register to simplify software design.
- Single +5 volt power supply.
- Serial echo mode.
- False start bit detection.
- 8-bit bi-directional data bus for direct communication with the microprocessor.
- External 16x clock input for non-standard baud rates (up to 125 Kbaud).
- Programmable: word lengths; number of stop bits; and parity bit generation and detection.
- Data set and modem control signals provided.
- Parity: (odd, even, none, mark, space).
- Full-duplex or half-duplex operation.
- 5, 6, 7, 8 and 9 bit transmission.

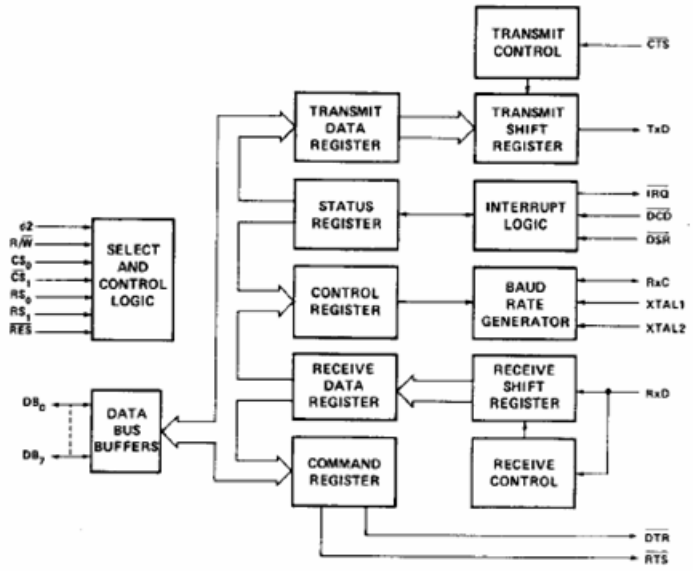
Description

The SY6551 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

Pin Configuration



Block Diagram



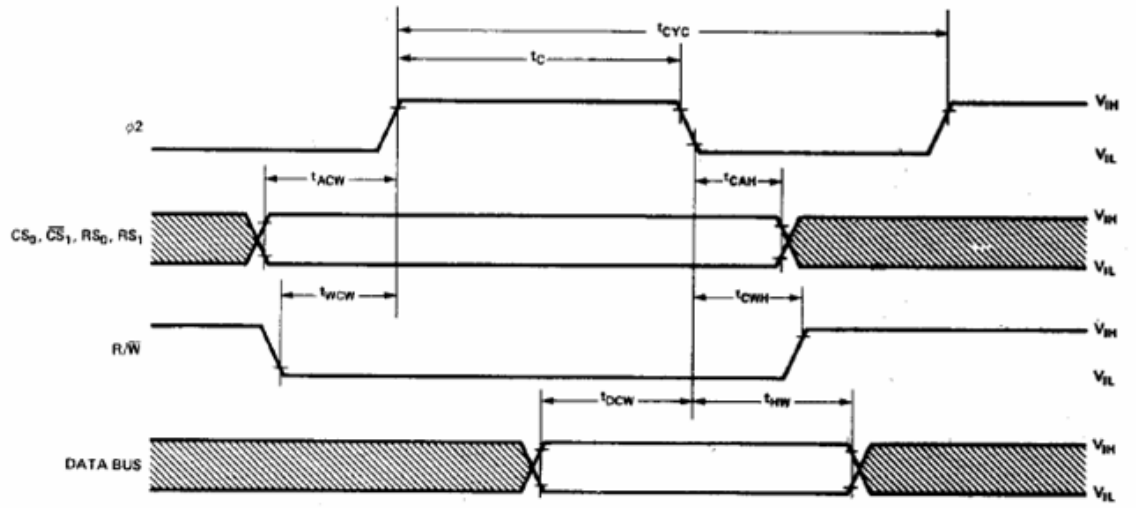


Figure 2. Write Timing Characteristics

Write Cycle (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Cycle Time	t_{CYC}	1.0	–	0.5	–	µs
$\phi 2$ Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACW}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCW}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns

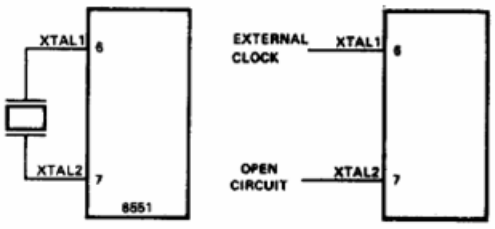
(t_r and t_f = 10 to 30 ns)

Crystal Specification

1. Temperature stability ± 0.01% (0° to 70°C)
2. Characteristics at 25°C ± 2°C
   a. Frequency (MHz) 1.8432
   b. Frequency tolerance (±%) 0.02
   c. Resonance mode Series
   d. Equivalent resistance (ohm) 400 max.
   e. Drive level mW 2
   f. Shunt capacitance pF 7 max.
   g. Oscillation mode Fundamental

No other external components should be in the crystal circuit

Clock Generation



INTERNAL CLOCK EXTERNAL CLOCK

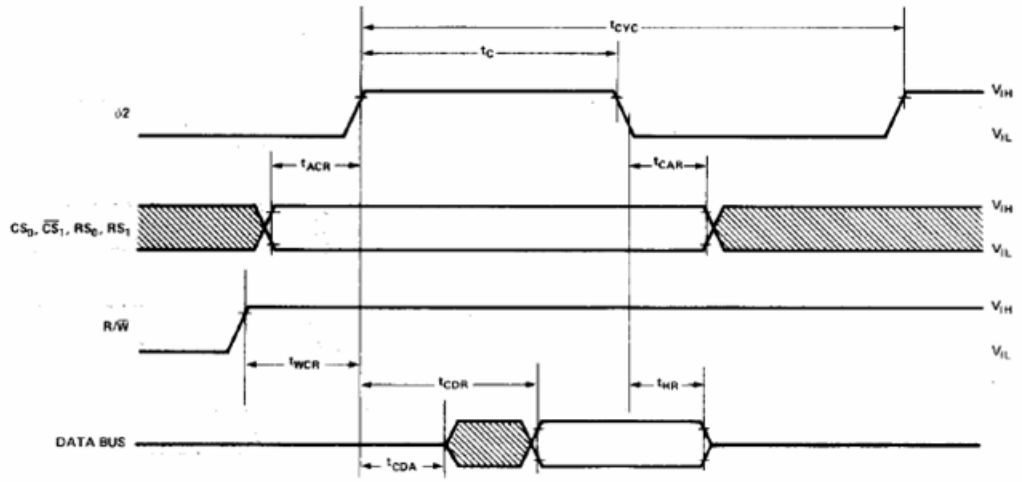


Figure 3. Read Timing Characteristics

Read Cycle (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	SY6551		SY6551A		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	–	0.5	–	μs
Pulse Width (ϕ2)	t_C	400	–	200	–	ns
Address Set-Up Time	t_{ACR}	120	–	70	–	ns
Address Hold Time	t_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WCR}	120	–	70	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Data Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

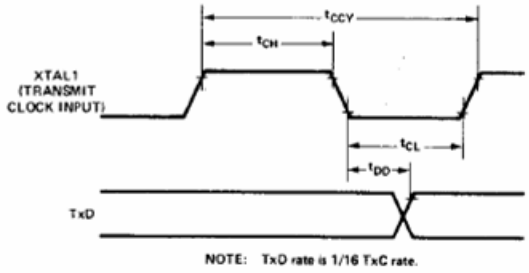


Figure 4a. Transmit Timing with External Clock

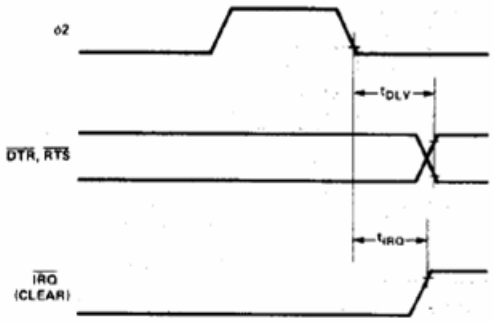


Figure 4b. Interrupt and Output Timing

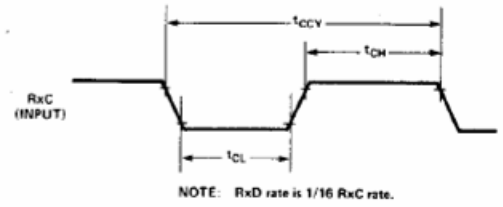


Figure 4c. Receive External Clock Timing

Transmit/Receive Characteristics

Characteristic	Symbol	SY6551 Min	SY6551 Max	SY6551A Min	SY6551A Max	Unit
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTAL1 to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

(t_r, t_f = 10 to 30 ns input clocks only)

*The baud rate with external clocking is: $\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}$

Interface Signal Description

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

$\phi 2$ (Input Clock)

The input clock is the system $\phi 2$ clock and is used to trigger all data transfers between the system microprocessor and the SY6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the SY6551. A low on the R/$\overline{W}$ pin allows a write to the SY6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0 - DB_7 (Data Bus)

The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the SY6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0, $\overline{CS_1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The SY6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_ϕ, RS_1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various SY6551 internal registers. The following table indicates the internal register select coding:

RS_1	RS_0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the SY6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTAL1, XTAL2 (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the SY6551 to the modem. A low on $\overline{DTR}$ indicates the SY6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the SY6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

$\overline{DCD}$ (Data Carrier Detect)

The $\overline{DCD}$ input pin is used to indicate to the SY6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Note: If Command Register Bit 0 = 1 and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low for the Receiver to operate.

Internal Organization

The Transmitter/Receiver sections of the SY6551 are depicted by the block diagram in Figure 5.

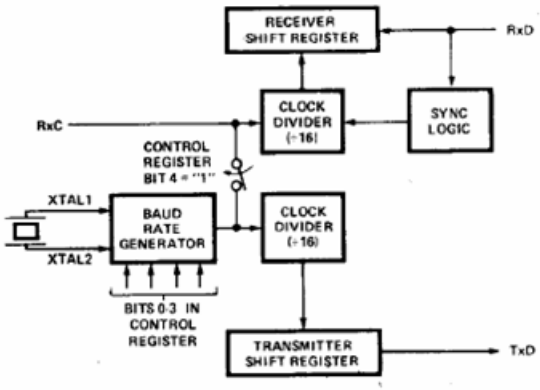


Figure 5. Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the SY6551.

Control Register

The Control Register is used to select the desired mode for the SY6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 6.

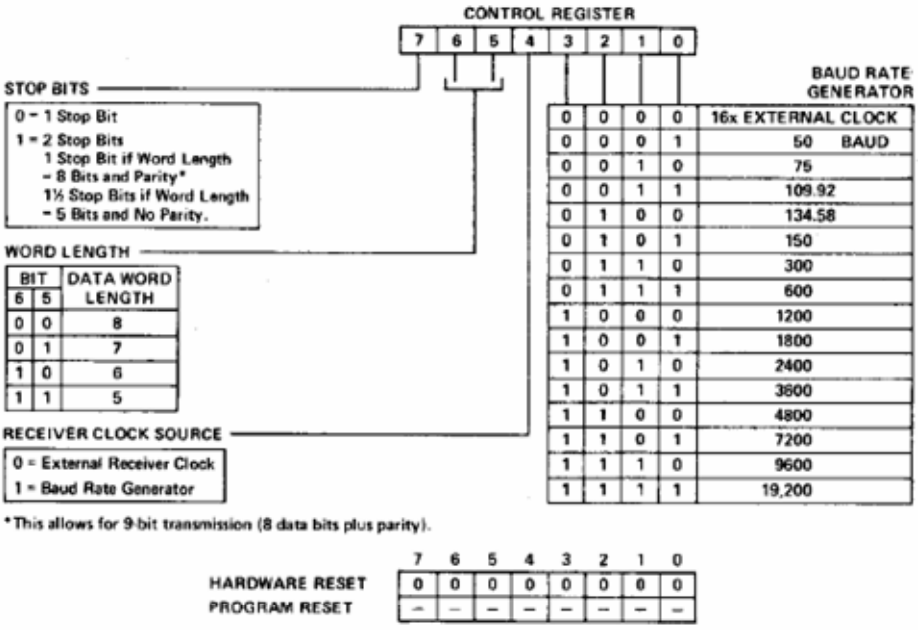
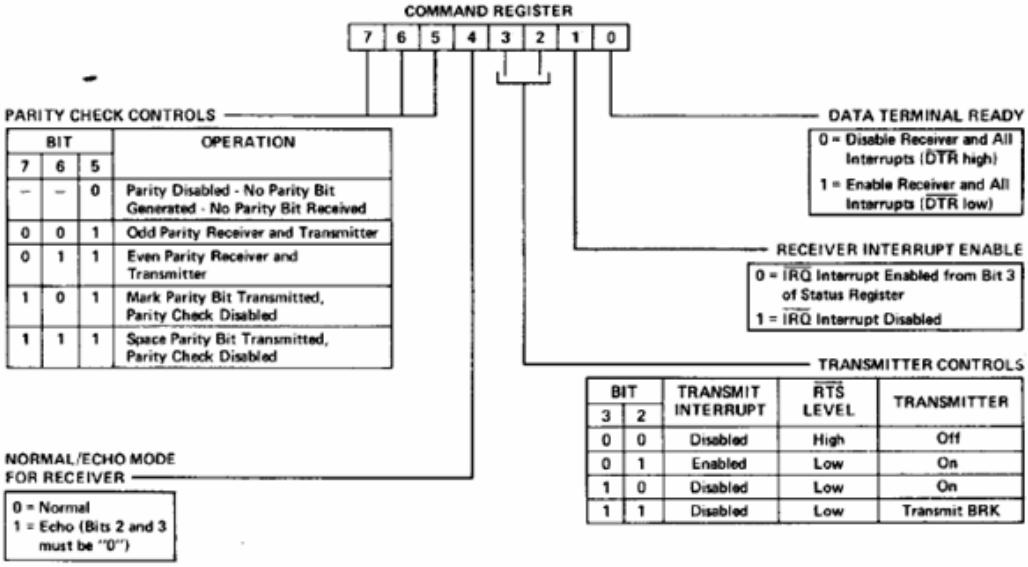


Figure 6. Control Register Format

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 7.



BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

Figure 7. Command Register Format

Status Register

The Status Register is used to indicate to the processor the status of various SY6551 functions and is outlined in Figure 8.

STATUS	SET BY	CLEARED BY
Parity Error*	0 = No Error 1 = Error	Self Clearing**
Framing Error*	0 = No Error 1 = Error	Self Clearing**
Overrun*	0 = No Error 1 = Error	Self Clearing**
Receive Data Register Full	0 = Not Full 1 = Full	Read Receive Data Register
Transmit Data Register Empty	0 = Not Empty 1 = Empty	Write Transmit Data Register
$\overline{DCD}$	0 = $\overline{DCD}$ Low 1 = $\overline{DCD}$ High	Not Resettable Reflects $\overline{DCD}$ State
$\overline{DSR}$	0 = $\overline{DSR}$ Low 1 = $\overline{DSR}$ High	Not Resettable Reflects $\overline{DSR}$ State
IRQ	0 = No Interrupt 1 = Interrupt	Read Status Register

*NO INTERRUPT GENERATED FOR THESE CONDITIONS.
**CLEARED AUTOMATICALLY AFTER A READ OF RDR AND THE NEXT ERROR FREE RECEIPT OF DATA.

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	–	–	1	0	0	0	0
PROGRAM RESET	–	–	–	–	–	0	–	–

Figure 8. Status Register Format

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 9 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

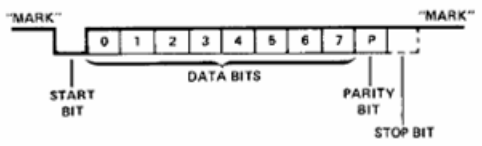
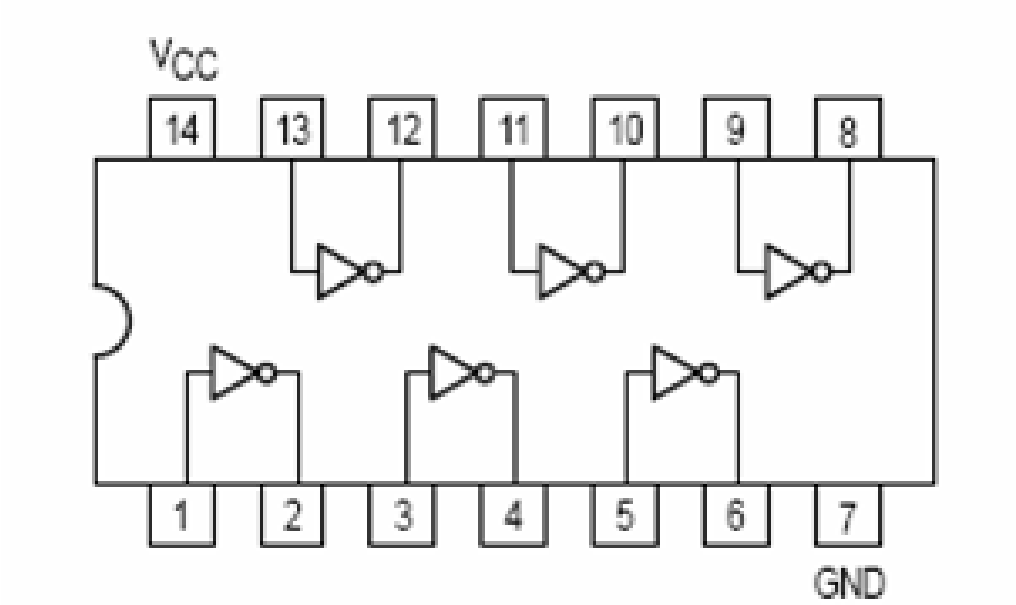
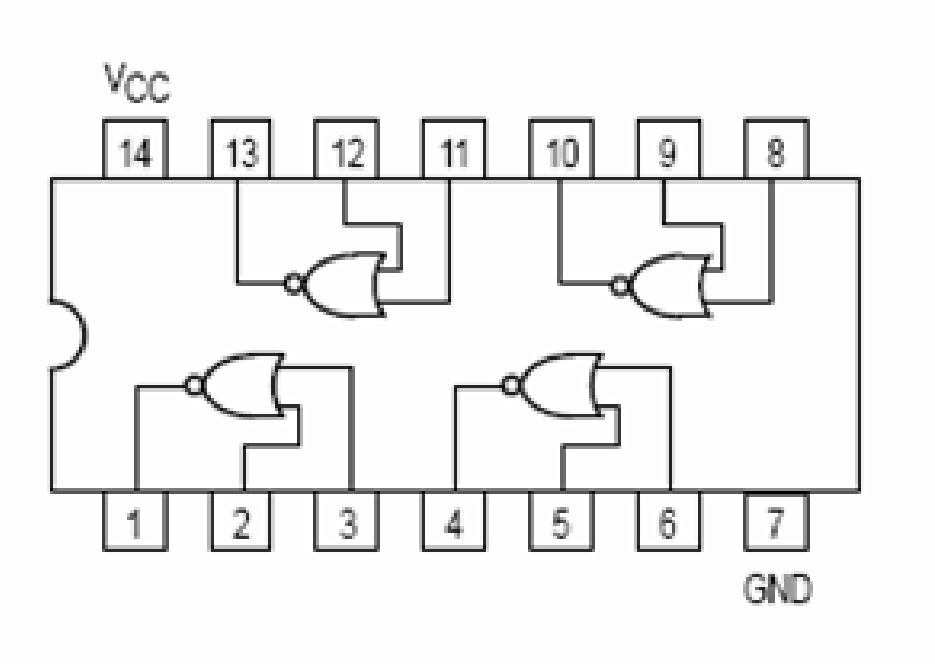


Figure 9. Serial Data Stream Example

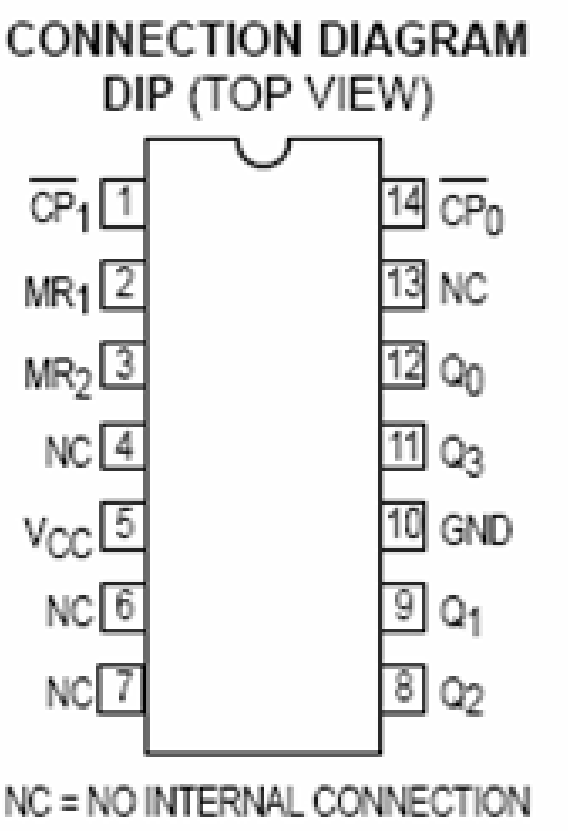
U7, U10
74LS04 HEX INVERTER

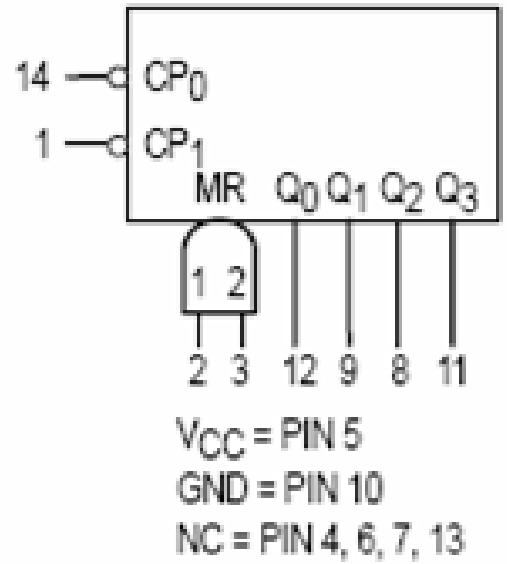


U8
74LS02 QUAD 2-INPUT NOR GATE



U9, U25
74LS93 4-BIT BINARY COUNTER



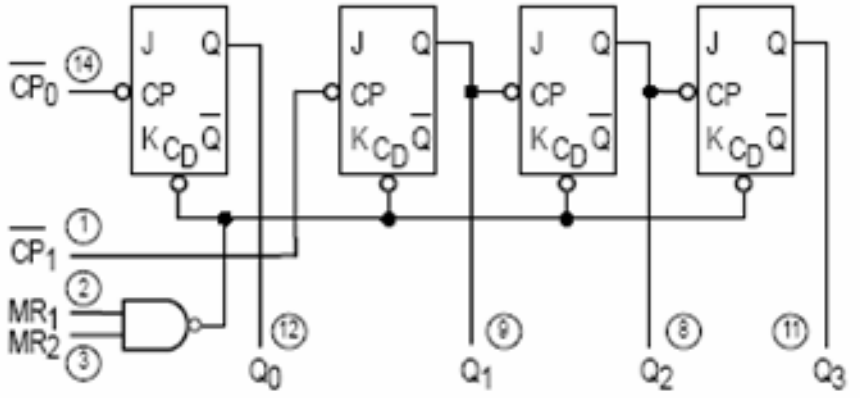


PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

LOGIC DIAGRAM

LS93



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 is connected to Input CP_1.

U11
74LS10 TRIPLE 3-INPUT NAND GATE

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A to 3A	data inputs
2, 4, 10	1B to 3B	data inputs
13, 5, 11	1C to 3C	data inputs
12, 6, 8	1Y to 3Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

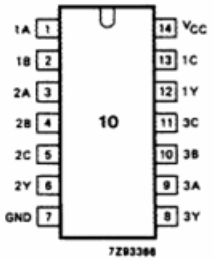


Fig.1 Pin configuration.

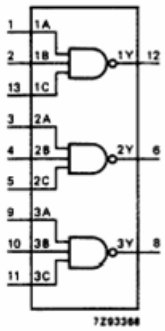


Fig.2 Logic symbol.

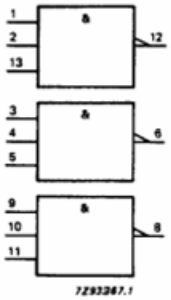


Fig.3 IEC logic symbol.

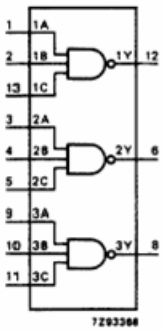


Fig.4 Functional diagram.

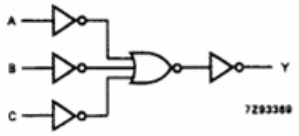


Fig.5 Logic diagram (one gate).

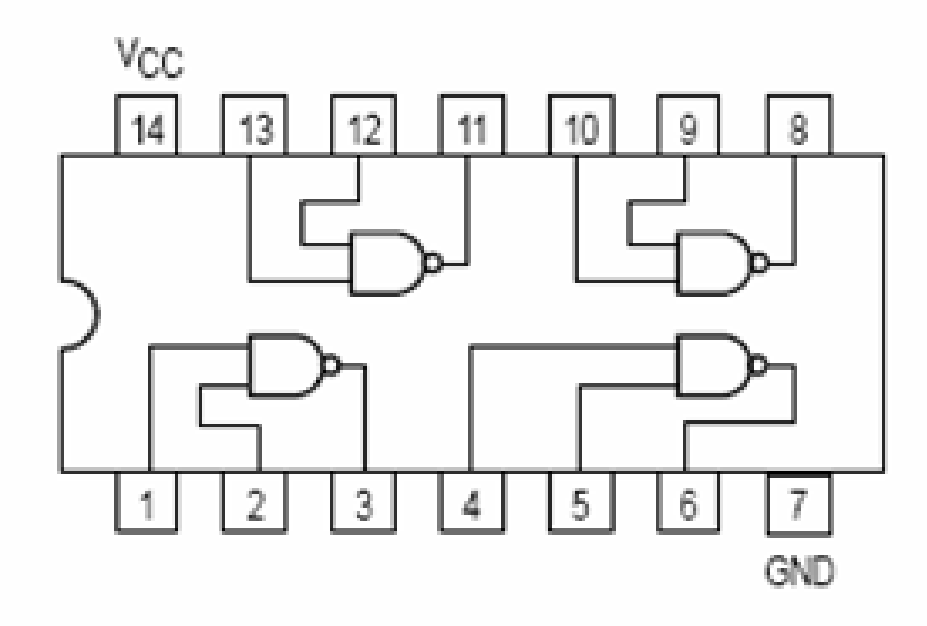
FUNCTION TABLE

INPUTS			OUTPUT
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

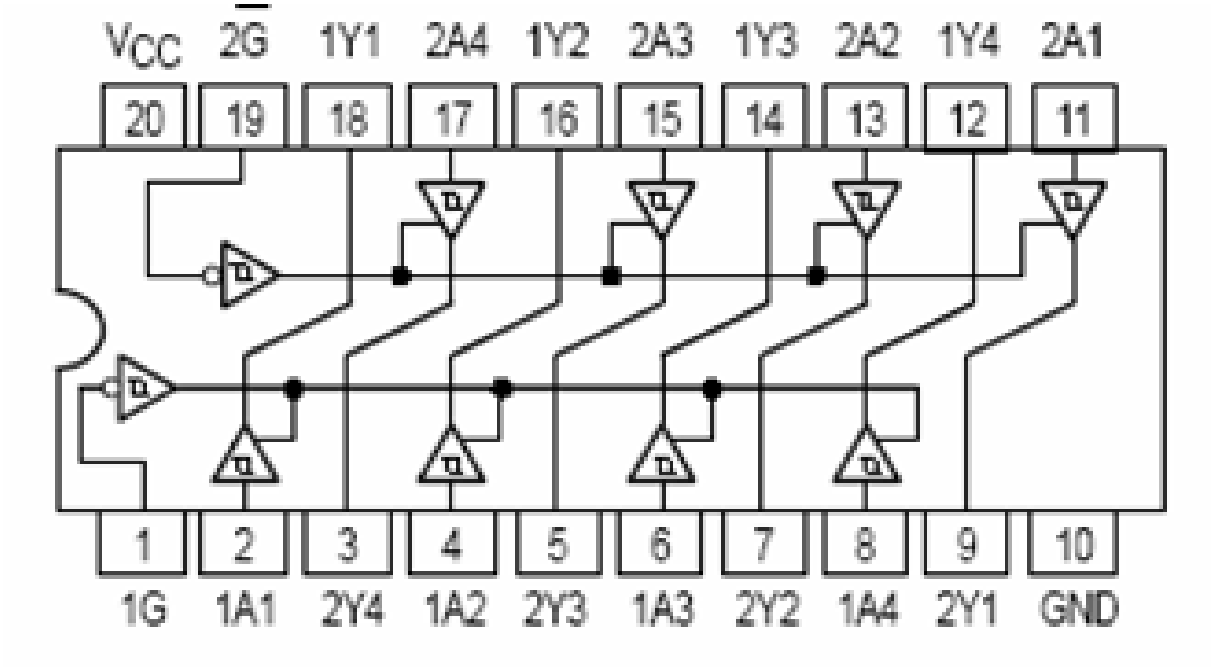
Notes

1. H = HIGH voltage level
   L = LOW voltage level

U13, U21, U67, U69
74LS00 QUAD 2-INPUT NAND GATE



U14, U26, U29, U49, U68
74LS244 OCTAL BUFFER/LINE DRIVER
WITH TRI-STATE OUTPUTS

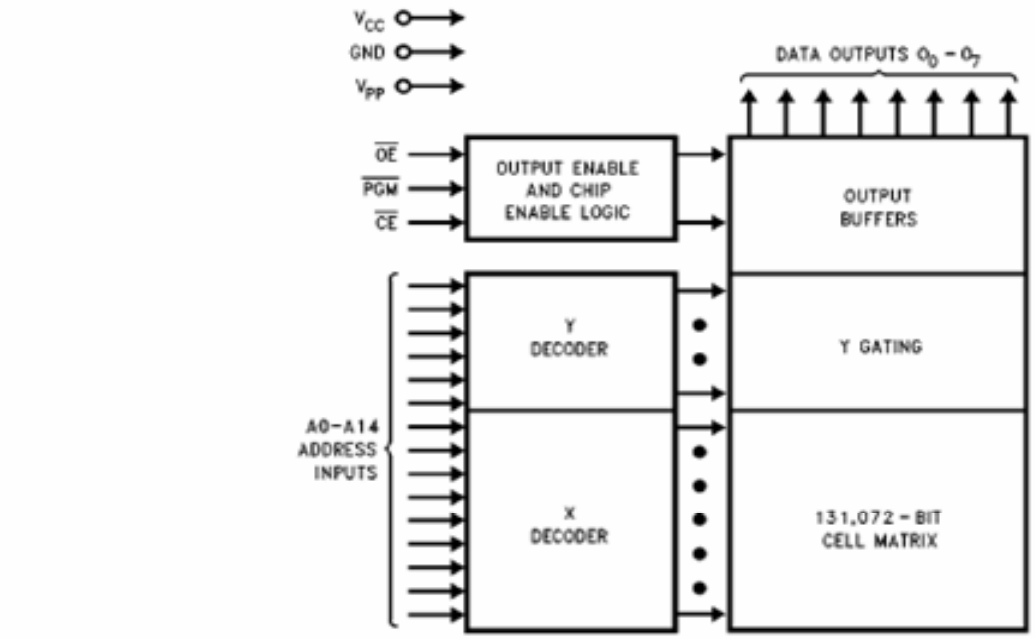


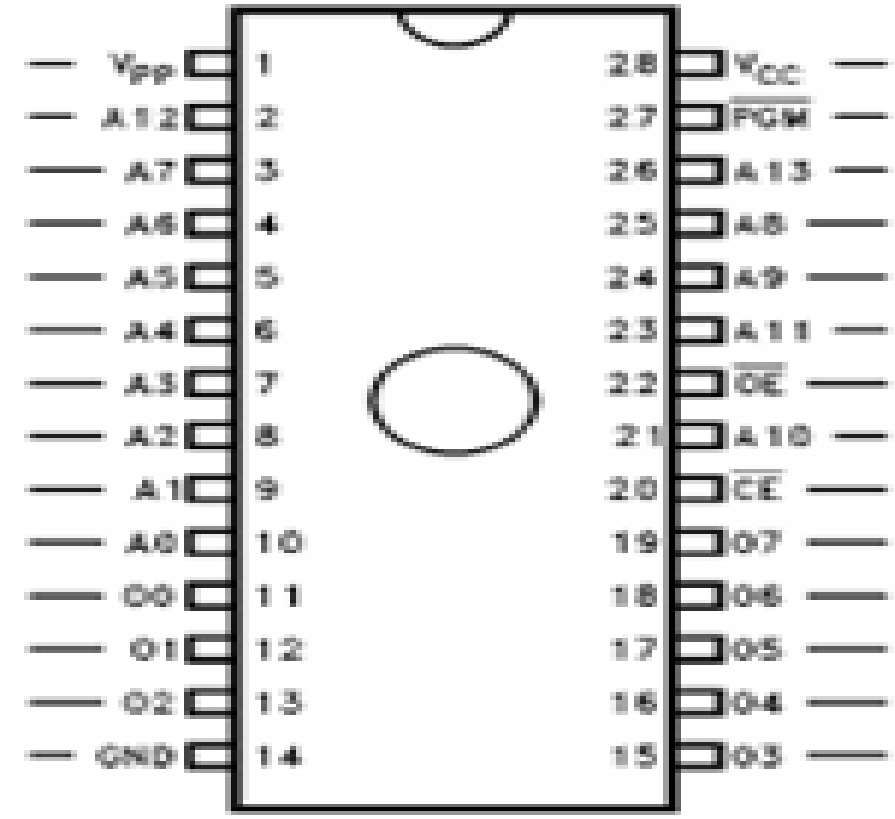
INPUTS		OUTPUT
1G, 2G	D	
L	L	L
L	H	H
H	X	(Z)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS241/244		12 12	18 18	ns

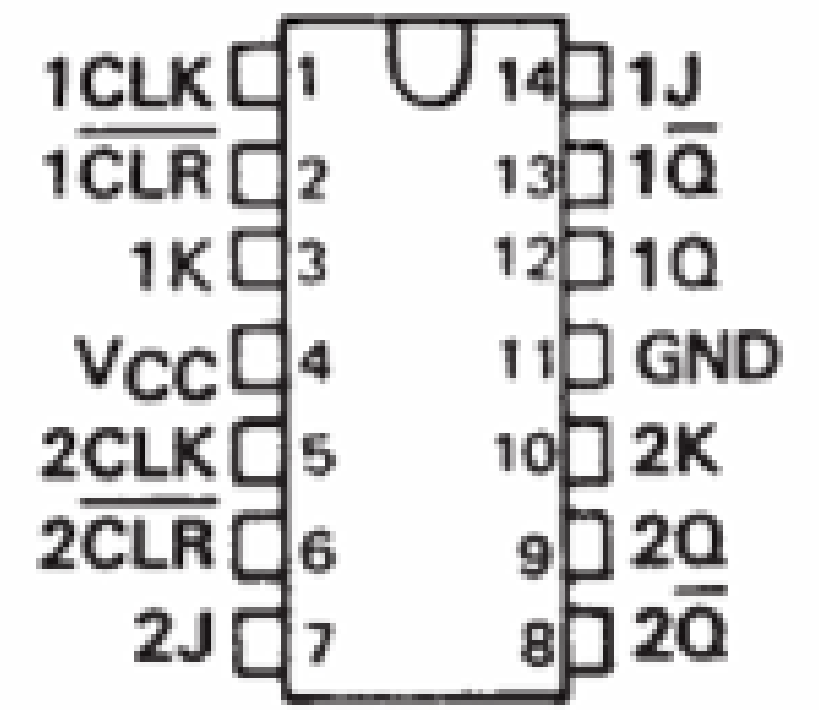
U15
27C128 16K x 8 EPROM

Block Diagram

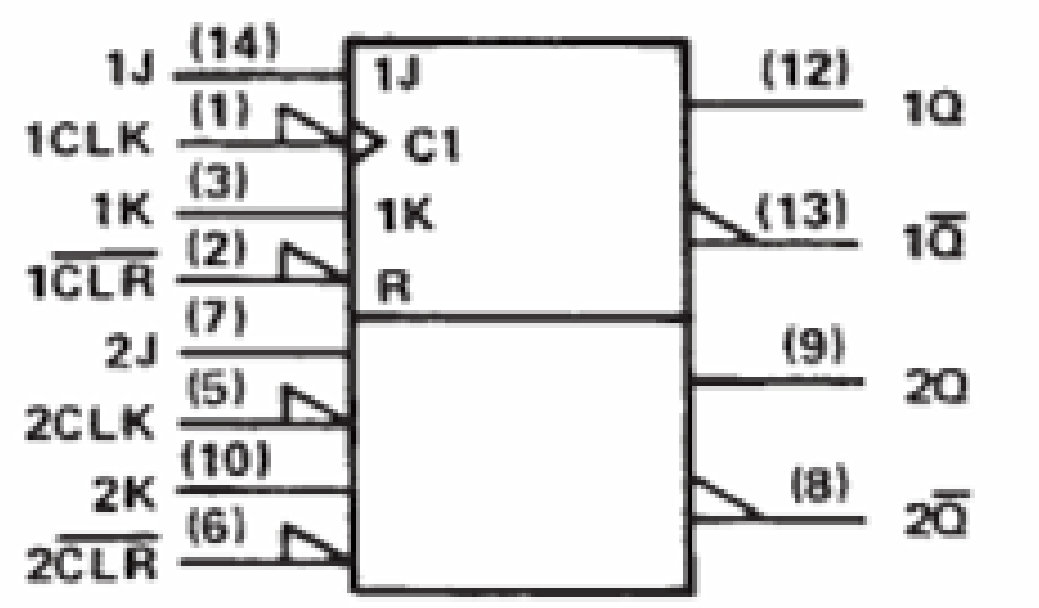


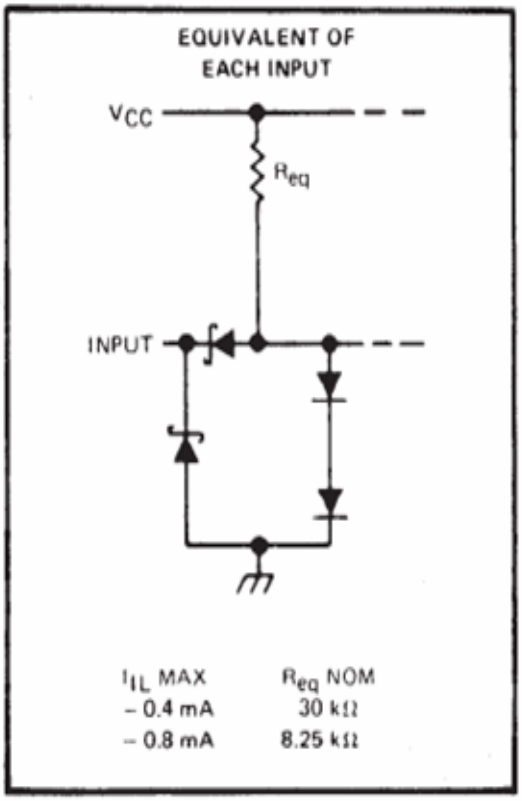


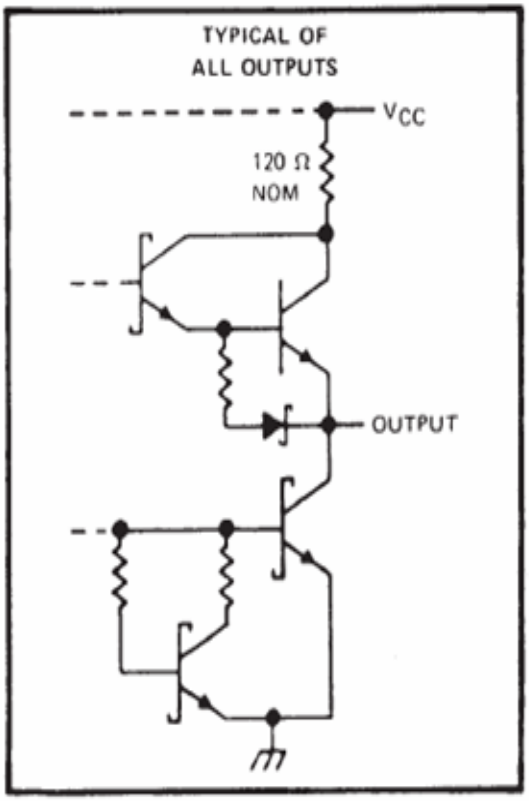
U16, U20
74LS73A DUAL J-K FLIP-FLOP
WITH CLEAR

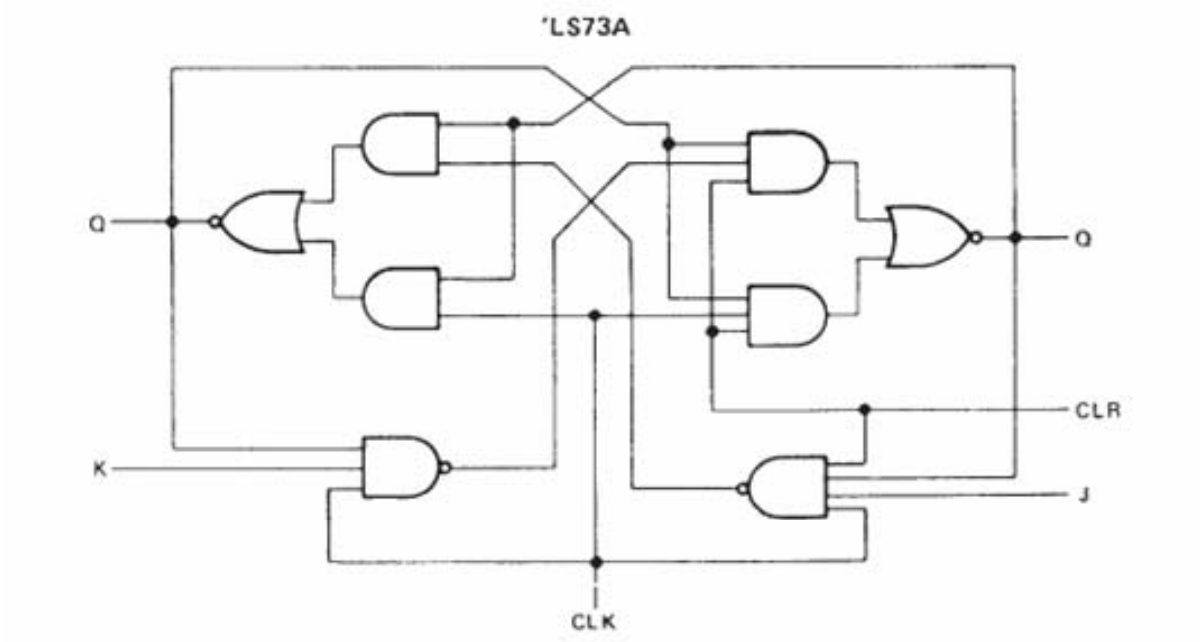


INPUTS				OUTPUTS	
$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_O	$\overline{Q}_O$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_O	$\overline{Q}_O$

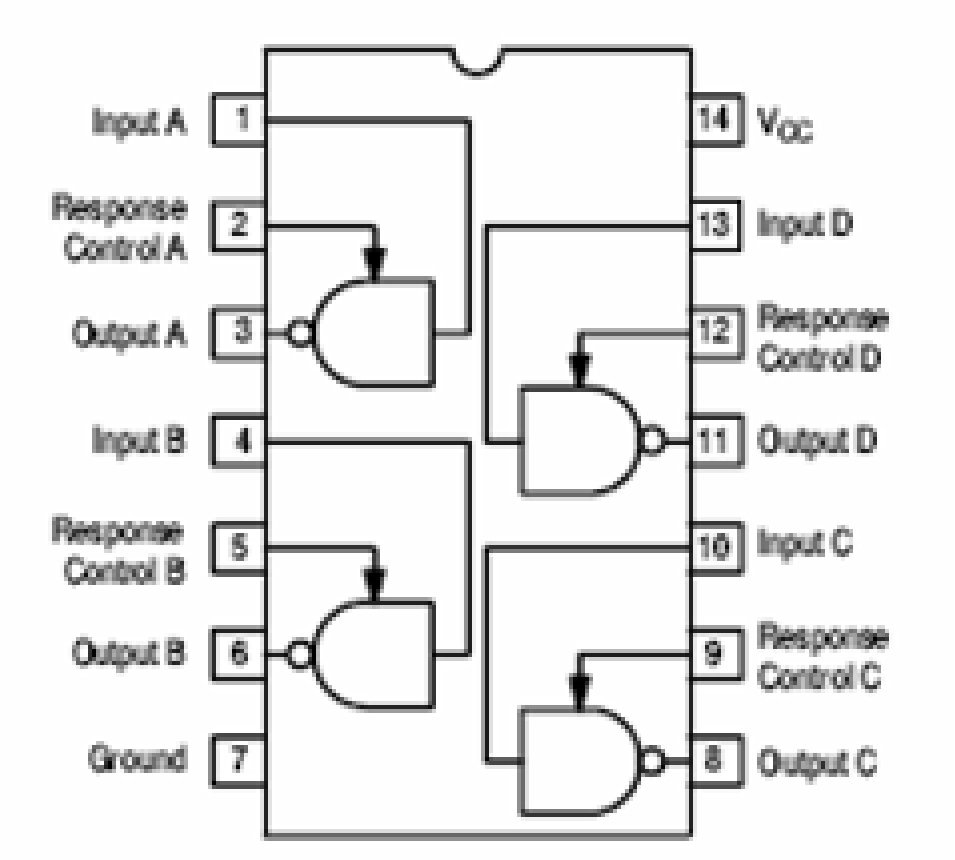

1J
(14)
1CLK
(1)
1K
(3)
1CLR
(2)
2J
(7)
2CLK
(5)
2K
(10)
2CLR
(6)
1J
C1
1K
R
(12)
1Q
(13)
1Q
(9)
2Q
(8)
2Q


EQUIVALENT OF
EACH INPUT
VCC
Req
INPUT
IIL MAX
– 0.4 mA
– 0.8 mA
Req NOM
30 kΩ
8.25 kΩ


TYPICAL OF
ALL OUTPUTS
VCC
120 Ω
NOM
OUTPUT


'LS73A
Q
Q
CLR
K
J
CLK

U17
MC1489P QUAD LINE RECIEVER



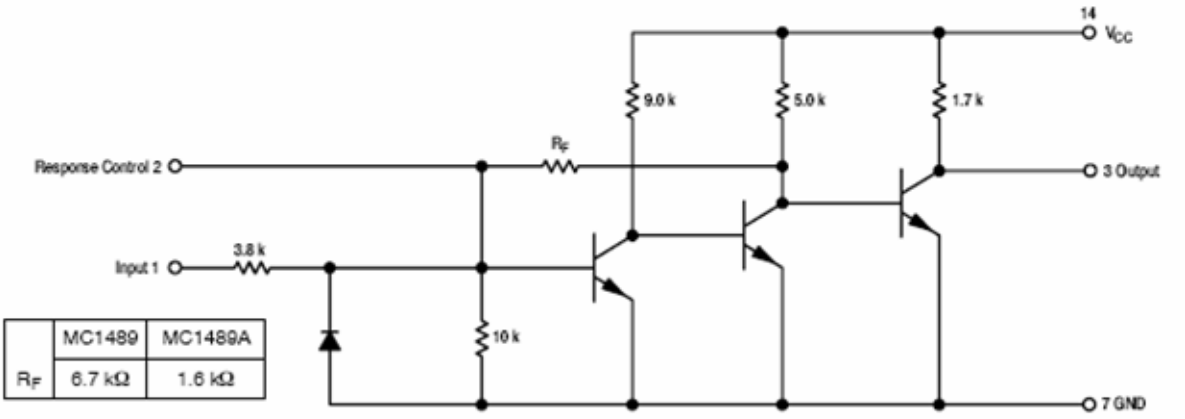
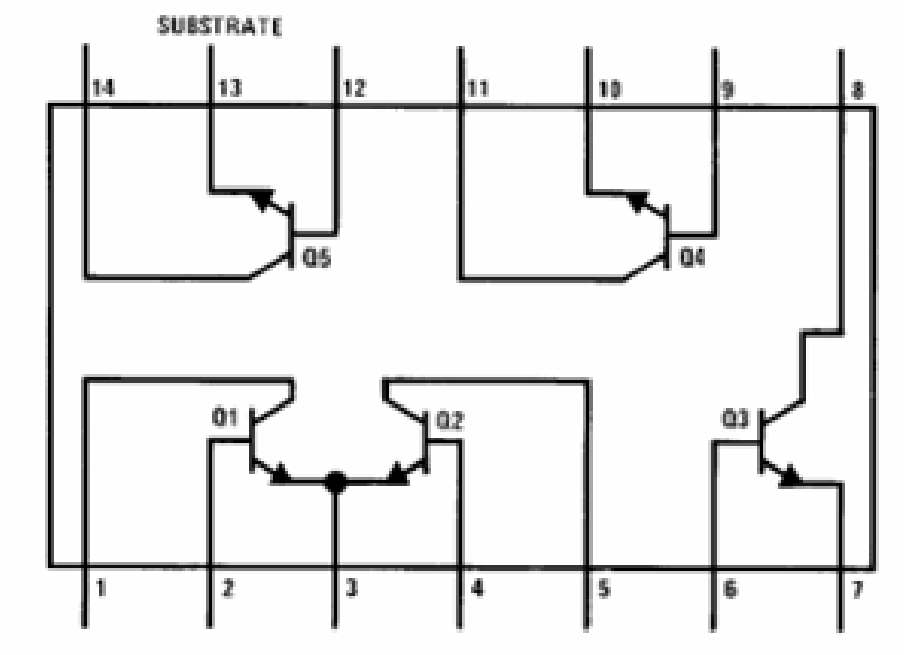
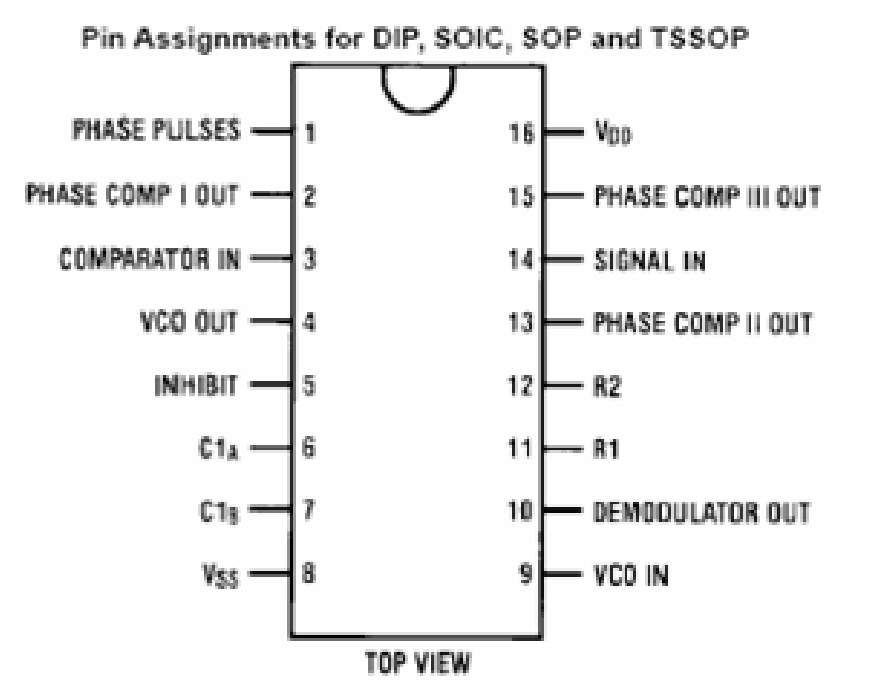


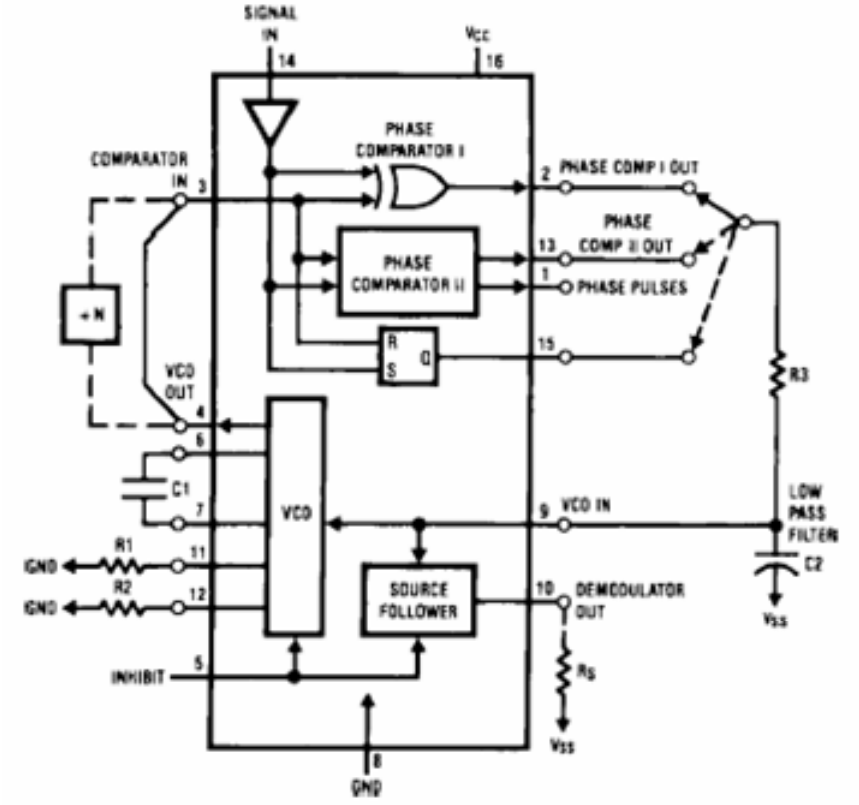
Figure 2. Representative Schematic Diagram
(1/4 of Circuit Shown)

U18
LM3086 TRANSISTOR ARRAY



U19
74HC4046 PHASE LOCKED LOOP



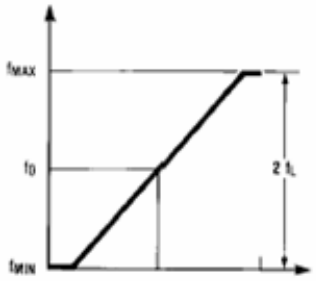


VOLTAGE CONTROLLED OSCILLATOR/SOURCE FOLLOWER

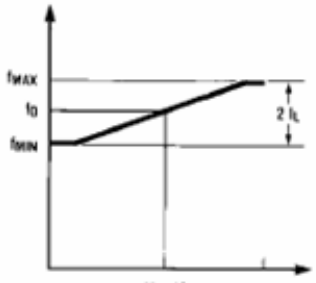
The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and capacitor C1 are selected to determine the center frequency of the VCO. R1 controls the lock range. As R1's resistance decreases the range of f_{MIN} to f_{MAX} increases. Thus the VCO's gain increases. As C1 is changed the offset (if used) of R2, and the center frequency is changed. (See typical performance curves) R2 can be used to set the offset frequency with 0V at VCO input. If R2 is omitted the VCO range is from 0Hz. As R2 is decreased the offset frequency is increased. The effect of R2 is shown in the design information table and typical performance curves. By increasing the value of R2 the lock range of the PLL is offset above 0Hz and the gain (Hz/Volt) does not change. In general, when offset is desired, R2 and C1 should be chosen first, and then R1 should be chosen to obtain the proper center frequency.

Internally the resistors set a current in a current mirror as shown in Figure 1. The mirrored current drives one side of the capacitor once the capacitor charges up to the threshold of the schmitt trigger the oscillator logic flips the capacitor over and causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to pin 4.

VCO WITHOUT OFFSET
R2 = ∞



VCO WITH OFFSET



Comparator I		Comparator II & III	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
•Given: f_0 •Use f_0 with curve titled center frequency vs R1, C to determine R1 and C1	•Given: f_0 and f_L •Calculate f_{MIN} from the equation $f_{MIN} = f_0 - f_L$ •Use f_{MIN} with curve titled offset frequency vs R2, C to determine R2 and C1 •Calculate f_{MAX}/f_{MIN} from the equation $f_{MAX}/f_{MIN} = f_0 + f_L/f_0 - f_L$ •Use f_{MAX}/f_{MIN} with curve titled f_{MAX}/f_{MIN} vs R2/R1 to determine ratio R2/R1 to obtain R1	•Given: f_{MAX} •Calculate f_0 from the equation $f_0 = f_{MAX}/2$ •Use f_0 with curve titled center frequency vs R1, C to determine R1 and C1	•Given: f_{MIN} and f_{MAX} •Use f_{MIN} with curve titled offset frequency vs R2, C to determine R2 and C1 •Calculate f_{MAX}/f_{MIN} •Use f_{MAX}/f_{MIN} with curve titled f_{MAX}/f_{MIN} vs R2/R1 to determine ratio R2/R1 to obtain R1

FIGURE 1.

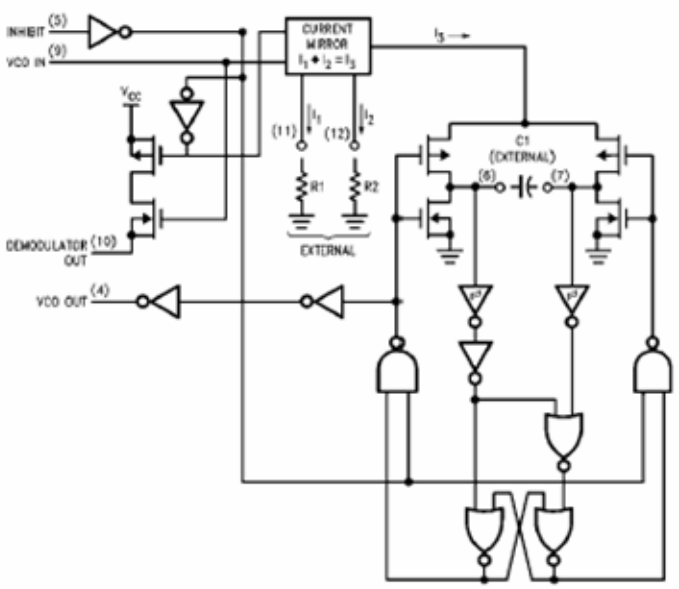


FIGURE 2. Logic Diagram for VCO

The input to the VCO is a very high impedance CMOS input and so it will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance a source follower transistor is provided. This transistor can be used by connecting a resistor to ground and its drain output will follow the VCO input signal.

An inhibit signal is provided to allow disabling of the VCO and the source follower. This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and source follower.

The output of the VCO is a standard high speed CMOS output with an equivalent LSTTL fanout of 10. The VCO output is approximately a square wave. This output can either directly feed the comparator input of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

PHASE COMPARATORS

All three phase comparators share two inputs, Signal In and Comparator In. The Signal In has a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then this input requires logic levels the same as standard 74HC. The Comparator input is a standard digital input. Both input structures are shown in Figure 3.

The outputs of these comparators are essentially standard 74HC voltage outputs. (Comparator II is 3-STATE.)

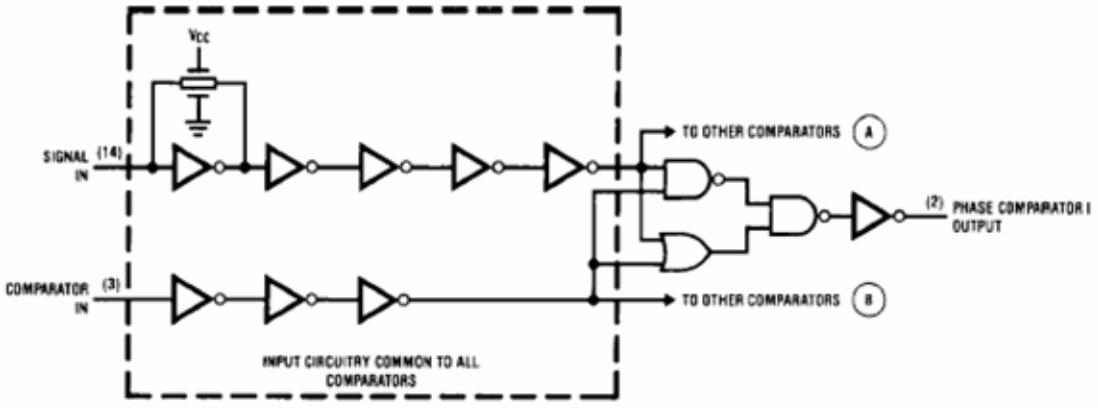


FIGURE 3. Logic Diagram for Phase Comparator I and the common input circuit for all three comparators

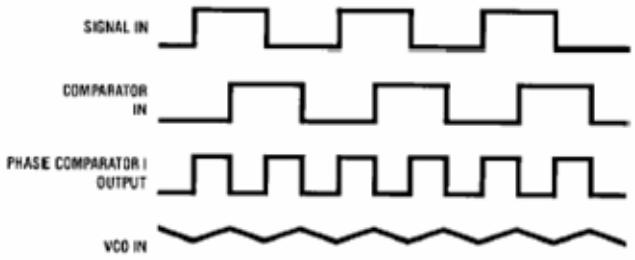


FIGURE 4. Typical Phase Comparator I. Waveforms

Thus in normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current output to the loop filter and this should be considered in the design. (The CD4046 also provides a voltage.)

Figure 5 shows the state tables for all three comparators.

PHASE COMPARATOR I

This comparator is a simple XOR gate similar to the 74HC86, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in Figure 4. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector I is dependent on the loop filter employed. The capture range can be as large as the lock range which is equal to the VCO frequency range.

To see how the detector operates refer to Figure 4. When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases the output duty cycle increases and the voltage after the loop filter increases. Thus in order to achieve lock, when the PLL input frequency increases the VCO input voltage must increase and the phase difference between comparator in and signal in will increase. At an input frequency equal f_{MIN}, the VCO input is at 0V and this requires the phase detector output to be ground hence the two input signals must be in phase. When the input frequency is f_{MAX} then the VCO input must be V_{CC} and the phase detector inputs must be 180° out of phase.

The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. This can be seen by noticing that a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to harmonics.

PHASE COMPARATOR II

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in Figure 6. This comparator acts only on the positive edges of the input signals and is thus independent of signal duty cycle.

Phase comparator II operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. Figure 7 shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector II output is set high. This will cause the loop filter to charge up the VCO input increasing the VCO frequency. Once the leading edge of the comparator input is detected the output goes 3-STATE holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

Phase Comparator State Diagrams

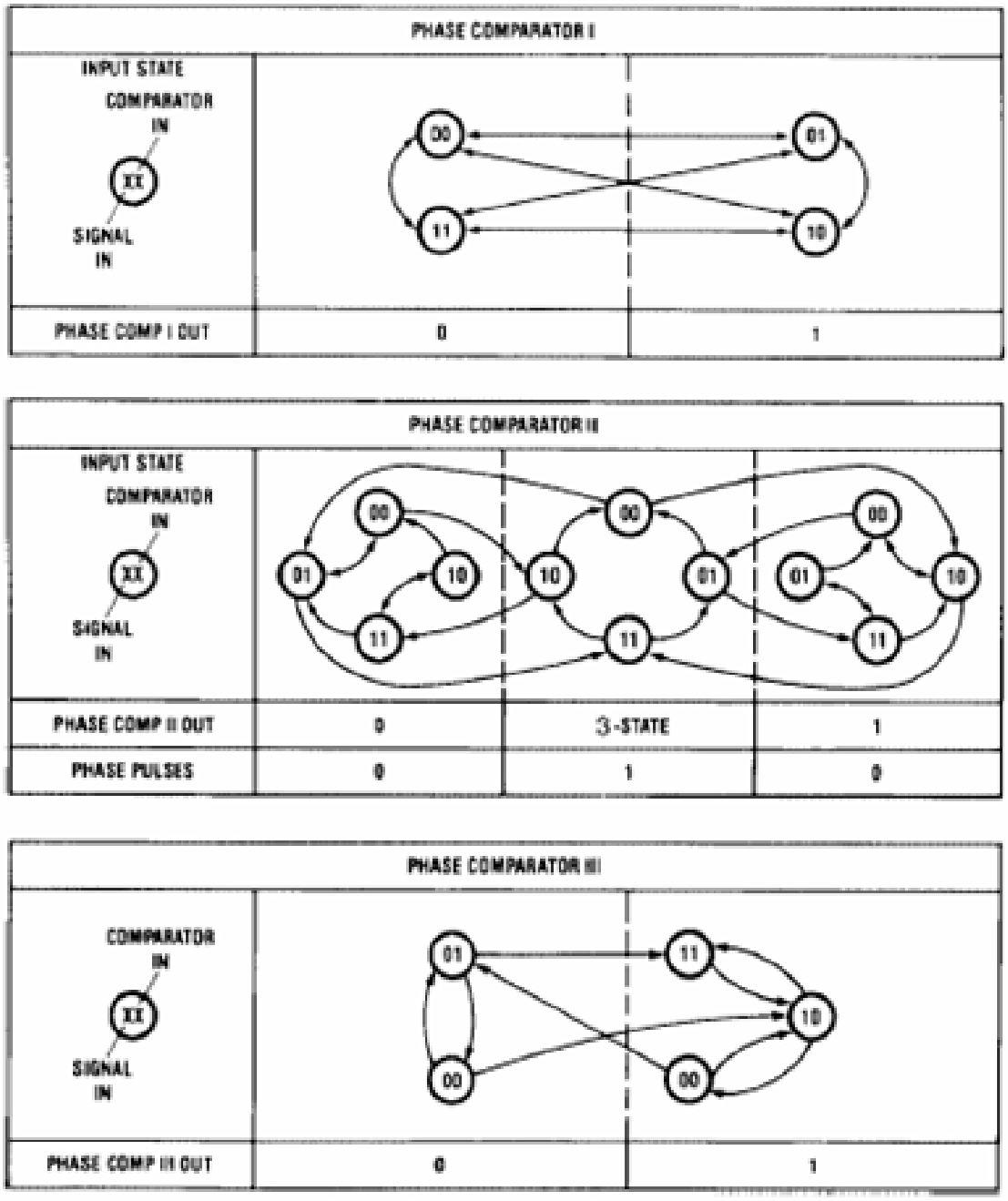


FIGURE 5. PLL State Tables

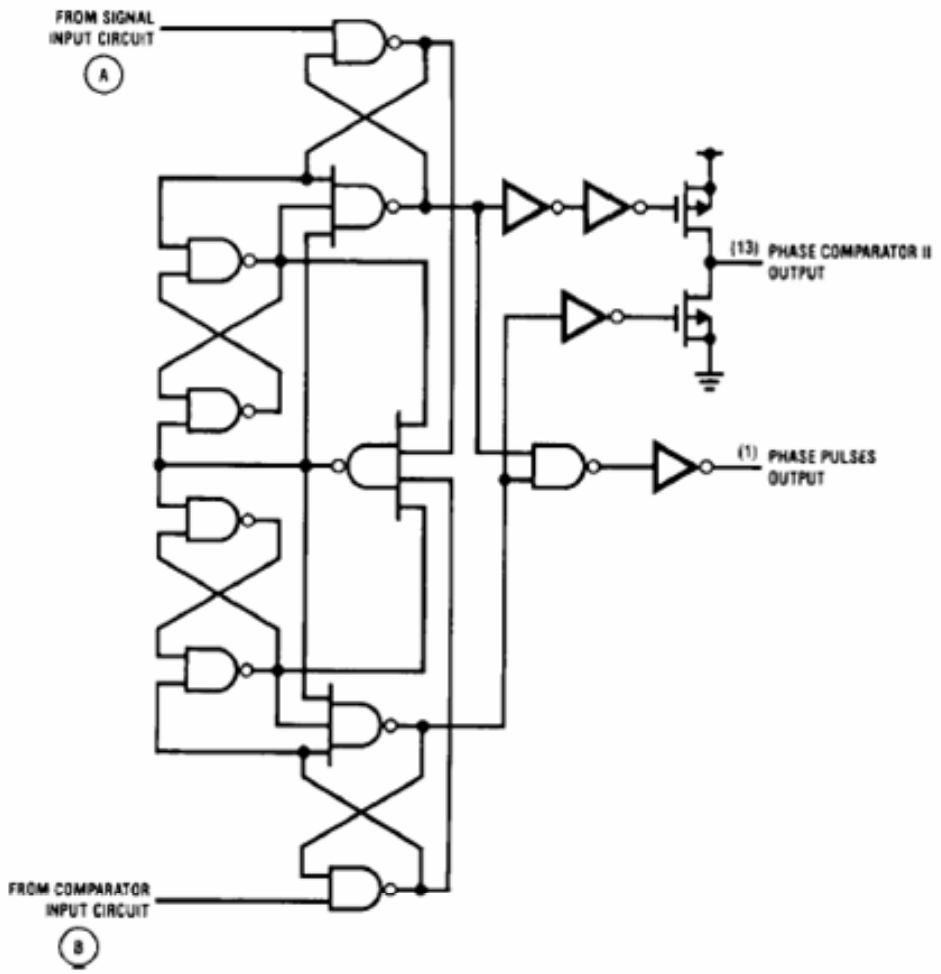


FIGURE 6. Logic Diagram for Phase Comparator II

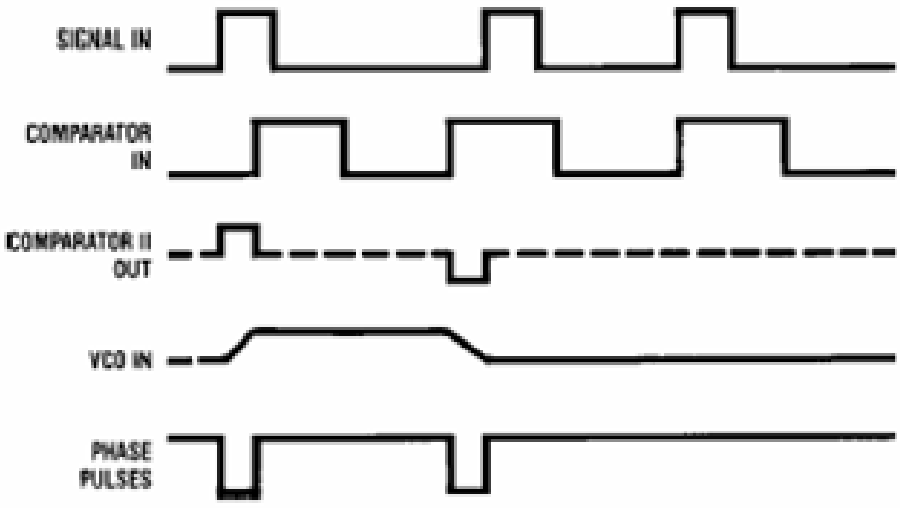


FIGURE 7. Typical Phase Comparator II Output Waveforms

Detailed Circuit Description (Continued)

If the VCO leads the signal then when the leading edge of the VCO is seen the output of the phase comparator goes LOW. This discharges the loop filter until the leading edge of the signal is detected at which time the output 3-STATE itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveform coincident.

When the PLL is out of lock the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be HIGH a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal the output of the detector will be LOW most of the time and the VCO's output frequency will be decreased.

As one can see when the PLL is locked the output of phase comparator II will be almost always 3-STATE except for minor corrections at the leading edge of the waveforms. When the detector is 3-STATE the phase pulse output is HIGH. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range. Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also when no signal is present the detector will see only VCO leading edges, and so the comparator output will stay LOW forcing the VCO to f_{MIN} operating frequency.

Phase comparator II is more susceptible to noise causing the phase lock loop to unlock. If a noise pulse is seen on the signal input, the comparator treats it as another positive edge of the signal and will cause the output to go HIGH until the VCO leading edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator I the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

PHASE COMPARATOR III

This comparator is a simple S-R Flip-Flop which can function as a phase comparator Figure 8. It has some similar characteristics to the edge sensitive comparator. To see how this detector works assume input pulses are applied to the signal and comparator inputs as shown in Figure 9. When the signal input leads the comparator input the flop is set. This will charge up the loop filter and cause the VCO to speed up, bringing the comparator into phase with the signal input. When using short pulses as input this comparator behaves very similar to the second comparator. But one can see that if the signal input is a long pulse, the output of the comparator will be forced to a one no matter how many comparator input pulses are received. Also if the VCO input is a square wave (as it is) and the signal input is pulse then the VCO will force the comparator output LOW much of the time. Therefore it is ideal to condition the signal and comparator input to short pulses. This is most easily done by using a series capacitor.

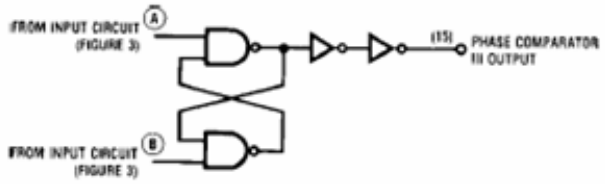


FIGURE 8. Phase Comparator III Logic Diagram

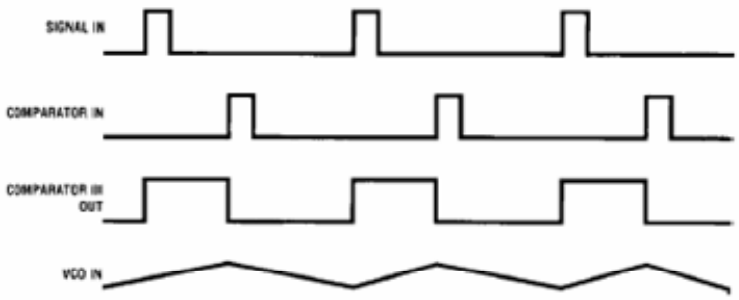
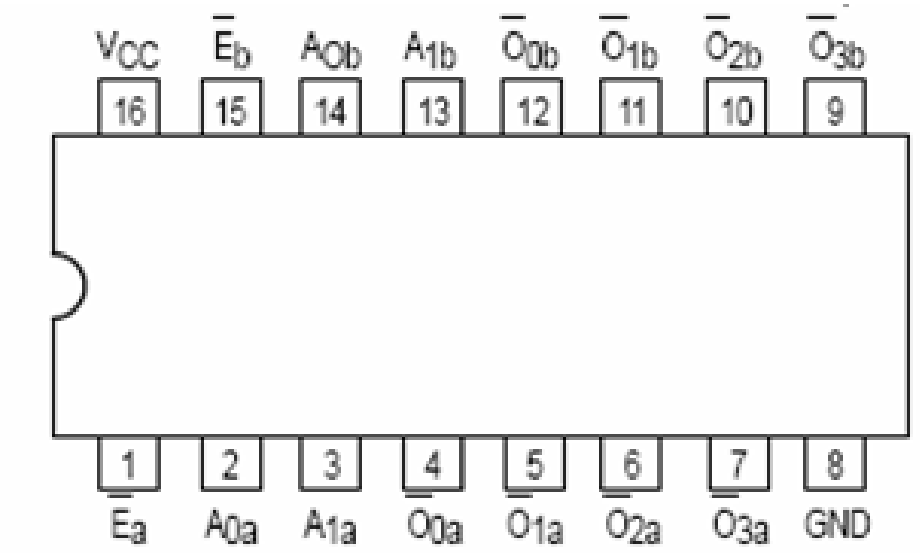


FIGURE 9. Typical Waveforms for Phase Comparator III

U22
74LS139 DUAL 1-OF-4 DECODER/DEMULTIPLEXER

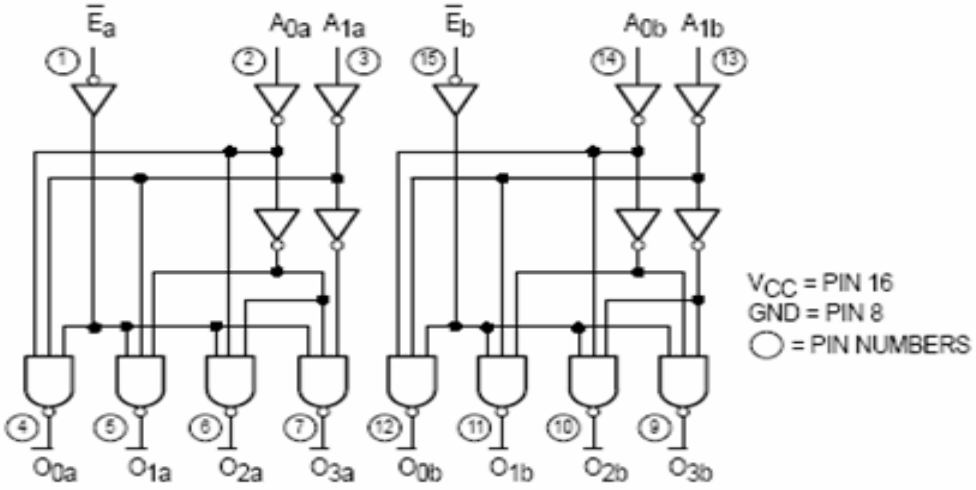


PIN NAMES

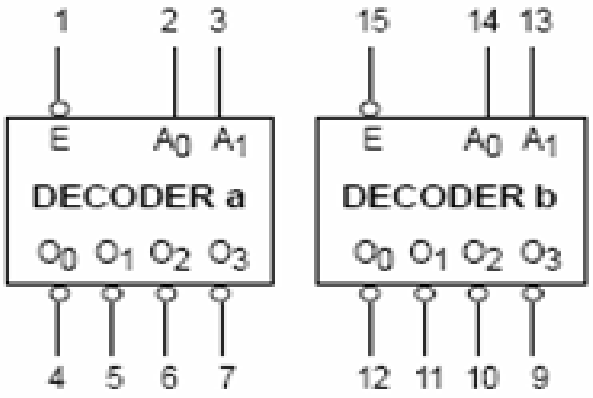
		LOADING (Note a) HIGH	LOADING (Note a) LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{O}_0 - \overline{O}_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

FUNCTIONAL DESCRIPTION

The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($O_0 - O_3$). Each decoder has an active LOW Enable (E). When E is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

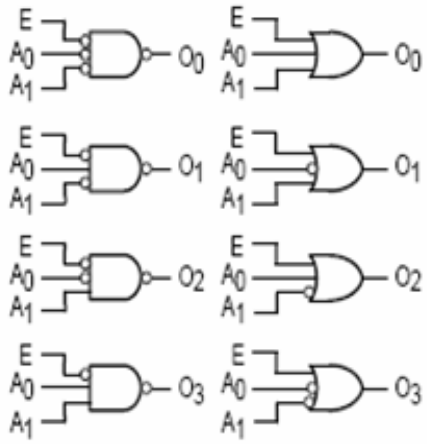
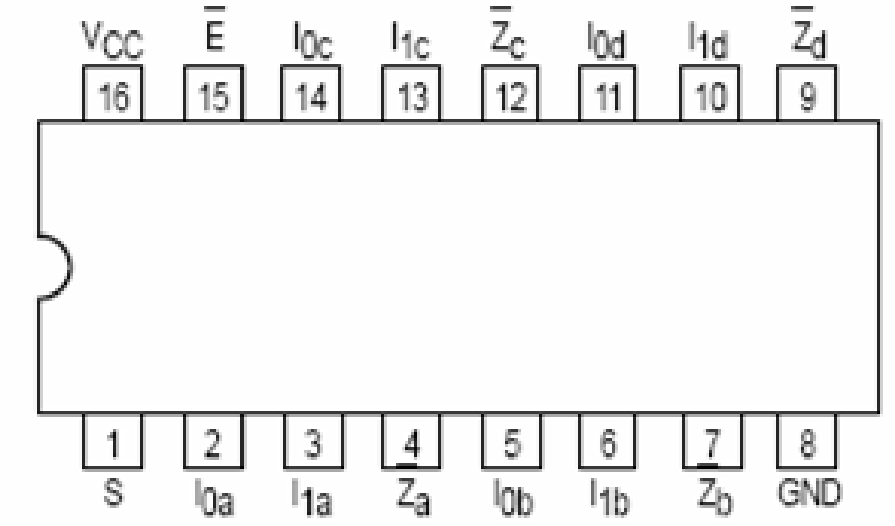


Figure a

U23
74LS158 QUAD 2-INPUT MULTIPLEXER

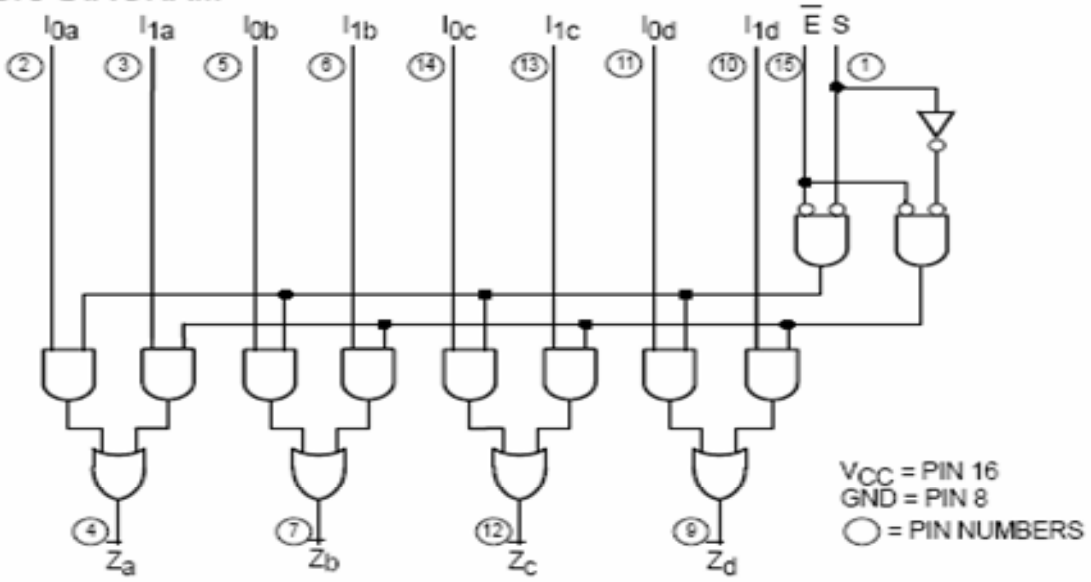


PIN NAMES

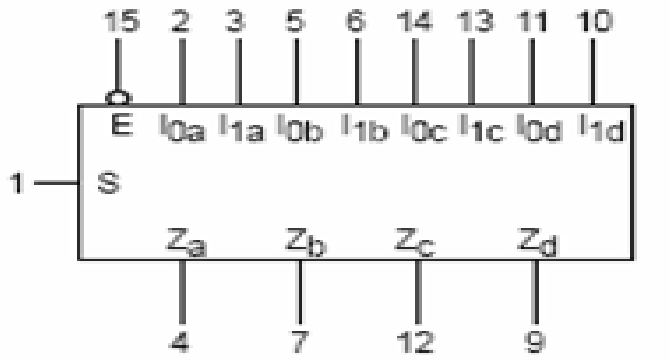
		LOADING (Note a)	
		HIGH	LOW
$\overline{S}$	Common Select Input	1.0 U.L.	0.5 U.L.
E	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$I_{0a}-I_{0d}$	Data Inputs from Source 0	0.5 U.L.	0.25 U.L.
$I_{1a}-I_{1d}$	Data Inputs from Source 1	0.5 U.L.	0.25 U.L.
Z_a-Z_d	Inverted Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

FUNCTIONAL DESCRIPTION

The LS158 is a Quad 2-input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S) and presents the data in inverted form at the four outputs. The Enable Input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced HIGH regardless of all other inputs.

The LS158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input.

A common use of the LS158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
E	S	I_0	I_1	Z
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

U27, U48
74LS374 OCTAL D-TYPE FLIP-FLOP; POSITIVE EDGE TRIGGER; TRI-STATE

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	3-state flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage

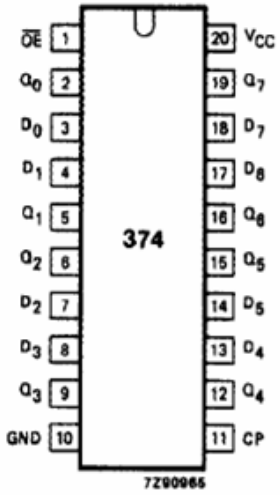


Fig.1 Pin configuration.

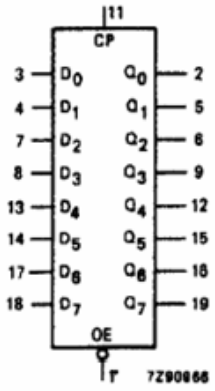


Fig.2 Logic symbol.

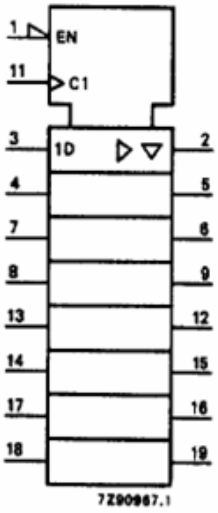


Fig.3 IEC logic symbol.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	13	ns
f_{max}	maximum clock frequency		77	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

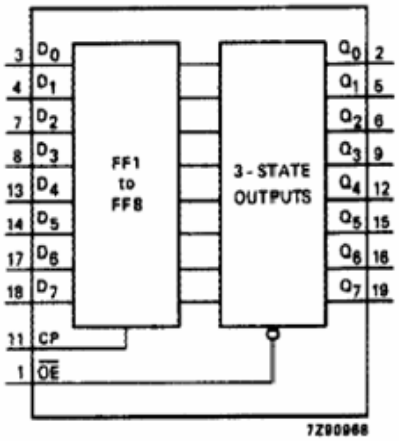


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   Z = high impedance OFF-state
   ↑ = LOW-to-HIGH CP transition

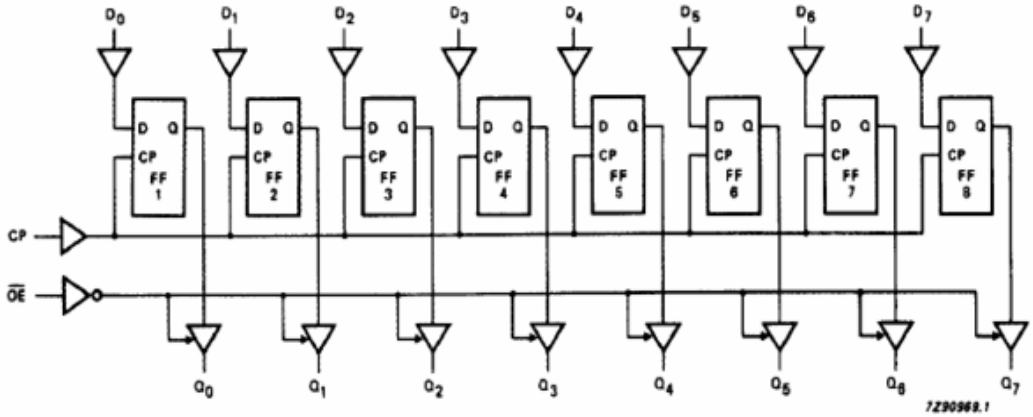
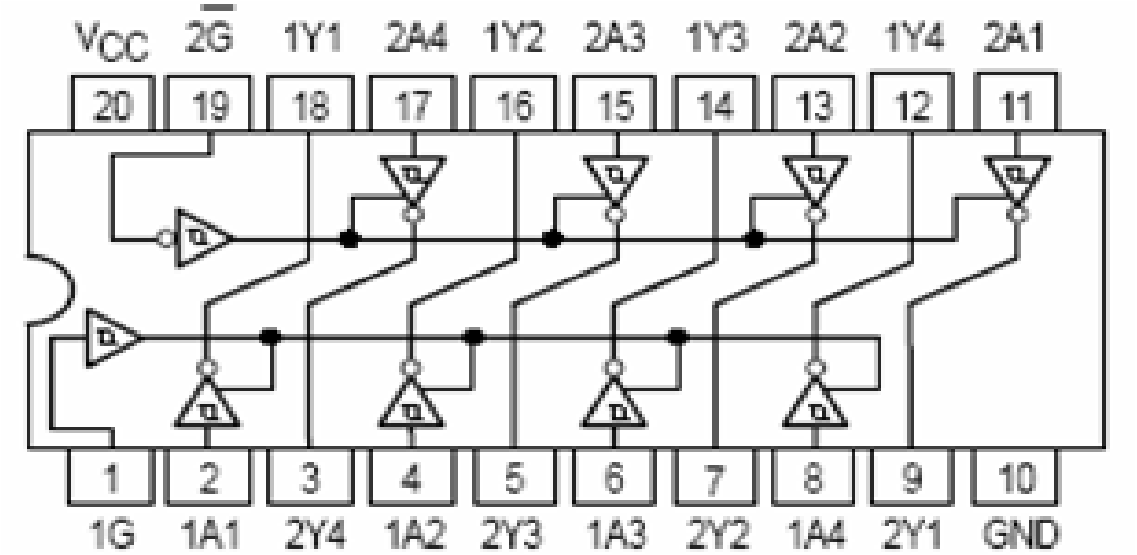


Fig.5 Logic diagram.

U28
74LS240 OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS



INPUTS		OUTPUT
1G, 2G	D	
L	L	H
L	H	L
H	X	(Z)

t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns

U47 MDP1603-330G
AND
U50 MDP1605 221/331G
DIP PACKAGE RESISTOR NETWORKS

Thick Film Resistor Networks, Dual-In-Line, Molded DIP, 01, 03, 05 Schematics

FEATURES

- 0.160" [4.06 mm] maximum seated height and rugged, molded case construction
- Thick film resistive elements
- Low temperature coefficient (- 55 °C to + 125 °C) ± 100 ppm/°C
- Reduces total assembly costs
- Compatible with automatic insertingbequipment
- Wide resistance range (10 Ω to 2.2 MΩ)
- Uniform performance characteristics
- Available in tube pack
- Lead (Pb)-free version is RoHS compliant

Pb Available

e1 RoHS* COMPLIANT

STANDARD ELECTRICAL SPECIFICATIONS

GLOBAL MODEL/ NO. OF PINS	SCHEMATIC	RESISTOR POWER RATING Max. AT 70 °C W	RESISTANCE RANGE Ω	STANDARD TOLERANCE ± %	TEMPERATURE COEFFICIENT (- 55 °C to + 125 °C) ppm/°C	TCR TRACKING** (- 55 °C to + 125 °C) ppm/°C	WEIGHT g
MDP 14	01 03 05	0.125 0.250 0.125	10 - 2.2M 10 - 2.2M Consult factory	± 2 (± 1, ± 5)***	± 100	± 50 ± 50 ± 100	1.3
MDP 16	01 03 05	0.125 0.250 0.125	10 - 2.2M 10 - 2.2M Consult factory	± 2 (± 1, ± 5)***	± 100	± 50 ± 50 ± 100	1.5

* For resistor power ratings at + 25 °C see derating curves
** Tighter tracking available
*** ± 1 % and ± 5 % tolerences available on request

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: MDP1403100RGD04 (preferred part numbering format)

M	D	P	1	4	0	3	1	0	0	R	G	D	0	4			

GLOBAL MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING	SPECIAL
MDP	14 = 14 Pin 16 = 16 Pin	01 = Bussed 03 = Isolated 00 = Special	R = Decimal K = Thousand M = Million 10R0 = 10 Ω 680K = 680 kΩ 1M00 = 1.0 MΩ	F = ± 1 % G = ± 2 % J = ± 5 % S = Special	E04 = Lead (Pb)-free, Tube D04 = Tin/Lead,Tube	Blank = Standard (Dash Number) (up to 3 digits) From 1-999 as applicable

Historical Part Number example: MDP1403101G (will continue to be accepted)

MDP	14	03	101	G	D04
HISTORICAL MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING

New Global Part Numbering: MDP1405121CGD04 (preferred part numbering format)

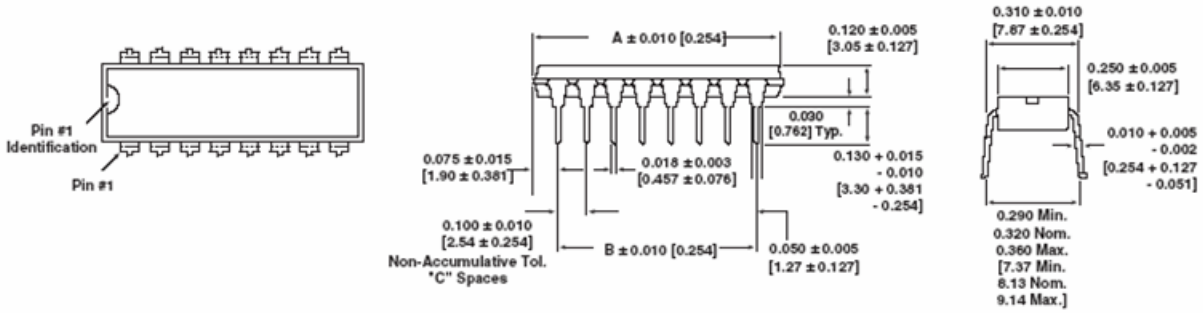
M	D	P	1	4	0	5	1	2	1	C	G	D	0	4			

GLOBAL MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE	TOLERANCE CODE	PACKAGING	SPECIAL
MDP	14 = 14 Pin 16 = 16 Pin	05 = Dual Terminator	3 digit Impedance code followed by Alpha modifier (see Impedence codes table)	F = ± 1 % G = ± 2 % J = ± 5 %	E04 = Lead (Pb)-free, Tube D04 = Tin/Lead,Tube	Blank = Standard (Dash Number) (up to 3 digits) From 1-999 as applicable

Historical Part Number example: MDP1405221271G (will continue to be accepted)

MDP	14	05	221	271	G	D04
HISTORICAL MODEL	PIN COUNT	SCHEMATIC	RESISTANCE VALUE 1	RESISTANCE VALUE 2	TOLERANCE CODE	PACKAGING

DIMENSIONS in inches [millimeters]



GLOBAL MODEL	A	B	C
MDP 14	0.750 [19.05]	0.600 [15.24]	6
MDP 16	0.850 [21.59]	0.700 [17.78]	7

TECHNICAL SPECIFICATIONS			
PARAMETER	UNIT	MDP14	MDP16
Package Power Rating (Maximum at + 70 °C)	W	1.73	1.92
Voltage Coefficient of Resistance	V_{eff}	< 50 ppm typical	
Dielectric Strength	VAC	200	
Insulation Resistance	Ω	> 10 000M minimum	
Operating Temperature Range	°C	- 55 to + 125	
Storage Temperature Range	°C	- 55 to + 150	

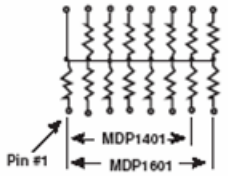
MECHANICAL SPECIFICATIONS	
Marking Resistance to Solvents:	Permanency testing per MIL-STD-202, Method 215
Solderability:	Per MIL-STD-202, Method 208E
Body:	Molded epoxy
Terminals:	Solder plated leads
Weight:	14 pin = 1.3 grams; 16 pin = 1.5 grams

IMPEDANCE CODES

CODE	R1(Ω)	R2(Ω)	CODE	R1(Ω)	R2(Ω)
500B	82	130	141A	270	270
750B	120	200	181A	330	390
800C	130	210	191A	330	470
990A	160	260	221B	330	680
101C	180	240	281B	560	560
111C	180	270	381B	560	1.2K
121B	180	390	501C	620	2.7K
121C	220	270	102A	1.5K	3.3K
131A	220	330	202B	3K	6.2K

CIRCUIT APPLICATIONS

01 SCHEMATIC

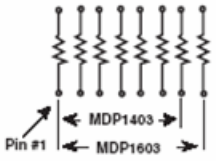


13 and 15 resistors with one pin common

The MDPXX01 circuit provides a choice of 13 and 15 nominally equal resistors, each connected between a common pin (14 and 16) and a discrete PC board pin. Commonly used in the following applications:

- MOS/ROM Pull-up/Pull-down
- Open Collector Pull-up
- "Wired OR" Pull-up
- Power Driven Pull-up
- TTL Input Pull-down
- Digital Pulse Squaring
- TTL Unused Gate Pull-up
- High Speed Parallel Pull-up

03 SCHEMATIC

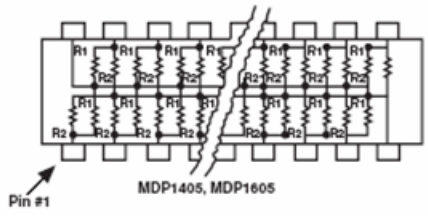


7 and 8 isolated resistors

The MDPXX03 provides a choice of 7 and 8 nominally equal resistors, each resistor isolated from all others and wired directly across. Commonly used in the following applications:

- "Wired OR" Pull-up
- Power Driven Pull-up
- Powergate Pull-up
- Line Termination
- Long-line Impedance Balancing
- LED Current Limiting
- ECL Output Pull-down
- TTL Input Pull-down

05 SCHEMATIC



TTL dual-line terminator; pulse squaring

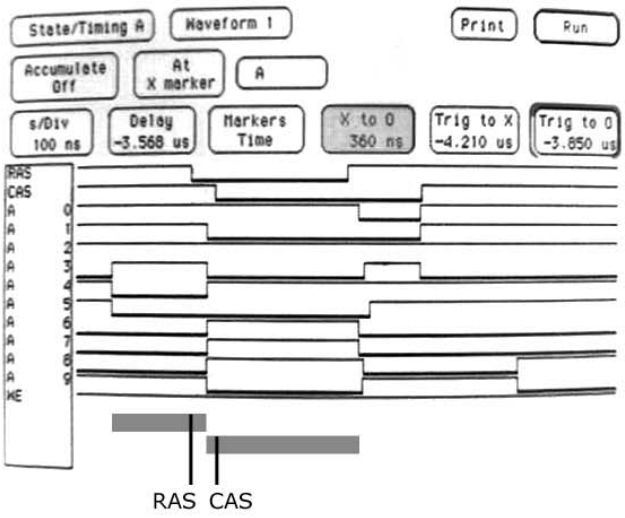
The MDPXX05 circuit contains 12 and 14 series pair of resistors. Each series pair is connected between ground and a common line. The junction of these resistor pairs is connected to the input terminals.

The 05 circuits are designed for TTL dual-line termination and pulse squaring.

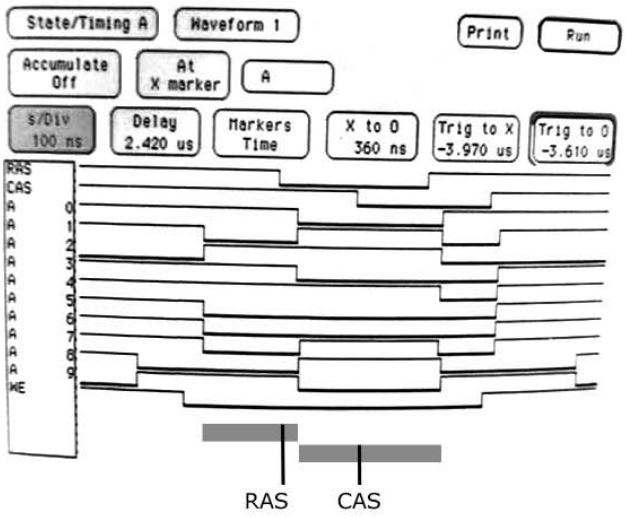
Standard E-24 resistance values stocked. Consult factory

MIO DRAM TIMING

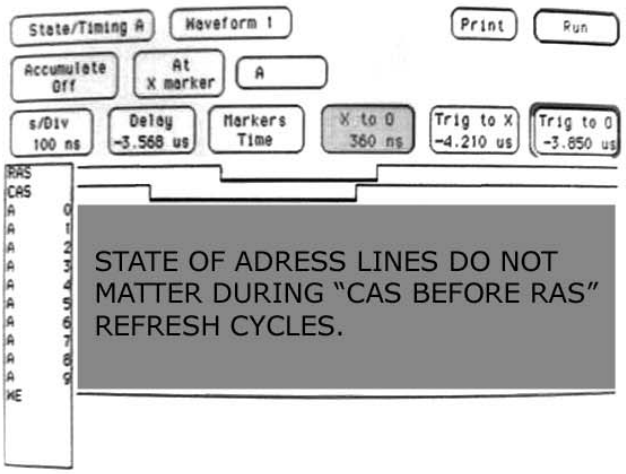
READ CYCLE



WRITE CYCLE



REFRESH CYCLE



DESIGN NOTES:

The 74LS244 at position U68 is used to create propogation delays on several circuits in order to bring timing characteristics of the MIO's DRAM control within acceptable ranges.

The RA8 and RA9 DRAM adress lines (indicated by A8 and A9 on the timing diagrams above) are each delayed by approximately 10ns. Each goes through a single buffer in U68.

The CAS circuit is delayed by approximately 40ns. This is done by using 4 buffers in U68, hooked in series.

The remaining 2 buffers in U68 are used to delay the signal that triggers the row adress setup by approximately 20ns. This line can be seen on the DRAM schematic comming from pin 3 of U13, going through U68 twice, and ending up at pins 1 and 19 of U14.

The "CAS before RAS" refresh scheme is used in order to avoid the need for extra counter circuitry which would be needed to generate 10 bits of refresh row adressing in the case of "RAS only" refresh.

Understanding the DRAM Timing Diagram

The most difficult aspect of working with DRAM devices is resolving the timing requirements. DRAMs are generally asynchronous, responding to input signals whenever they occur. As long as the signals are applied in the proper sequence, with signal durations and delays between signals that meet the specified limits, the DRAM will work properly.

The datasheets for our products contain timing diagrams for the particular devices. You may want to view a relevant timing diagram while reading the information below.

There are only a few signals that control the operation of a DRAM.

Row Address Select (Strobe) ($\overline{RAS}$) The $\overline{RAS}$ circuitry is used to latch the row address and to initiate the memory cycle. It is required at the beginning of every operation. $\overline{RAS}$ is active low; that is, to enable $\overline{RAS}$, a transition from a high voltage to a low voltage level is required. The voltage must remain low until $\overline{RAS}$ is no longer needed. During a complete memory cycle, there is a minimum amount of time that $\overline{RAS}$ must be active (t_{RAS}), and a minimum amount of time that $\overline{RAS}$ must be inactive, called the $\overline{RAS}$ precharge time (t_{RP}). $\overline{RAS}$ may also be used to trigger a refresh cycle ($\overline{RAS}$ Only Refresh, or ROR).

Column Address Select (Strobe) ($\overline{CAS}$) $\overline{CAS}$ is used to latch the column address and to initiate the read or write operation. $\overline{CAS}$ may also be used to trigger a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This refresh cycle requires $\overline{CAS}$ to be active prior to $\overline{RAS}$ and to remain active for a specified time. It is active low. The memory specification lists the minimum amount of time $\overline{CAS}$ must remain active (t_{CAS}) to initiate a read or write operation. For most memory operations, there is also a minimum amount of time that $\overline{CAS}$ must be inactive, called the $\overline{CAS}$ precharge time (t_{CP}). (An ROR cycle does not require $\overline{CAS}$ to be active.)

Address The addresses are used to select a memory location on the chip. The address pins on a memory device are used for both row and column address selection (multiplexing). The number of addresses depends on the memory's size and organization. The voltage level present at each address at the time that $\overline{RAS}$ or $\overline{CAS}$ goes active determines the row or column address, respectively, that is selected. To ensure that the row or column address selected is the one that was intended, set up and hold times with respect to the $\overline{RAS}$ and $\overline{CAS}$ transitions to a low level are specified in the DRAM timing specification.

Write Enable ($\overline{WE}$) The write enable signal is used to choose a read operation or a write operation. A low voltage level signifies that a write operation is desired; a high voltage level is used to choose a read operation. The operation to be performed is usually determined by the voltage level on $\overline{WE}$ when $\overline{CAS}$ goes low (Delayed Write is an exception). To ensure that the correct operation is selected, set up and hold times with respect to $\overline{CAS}$ are specified in the DRAM timing specification.

Output Enable ($\overline{OE}$) During a read operation, this control signal is used to prevent data from appearing at the output until needed. When $\overline{OE}$ is low, data appears at the data outputs as soon as it is available. $\overline{OE}$ is ignored during a write operation. In many applications, the $\overline{OE}$ pin is grounded and is not used to control the DRAM timing.

Data In or Out (DQs) The DQ pins (also called Input/Output pins or I/Os) on the memory device are used for input and output. During a write operation, a voltage (high=1, low=0) is applied to the DQ. This voltage is translated into the appropriate signal and stored in the selected memory cell. During a read operation, data read from the selected memory cell appears at the DQ once access is complete and the output is enabled ($\overline{OE}$ low). At most other times, the DQs are in a high impedance state; they do not source or sink any current, and do not present a signal to the system. This also prevents DQ contention when two or more devices share the data bus.

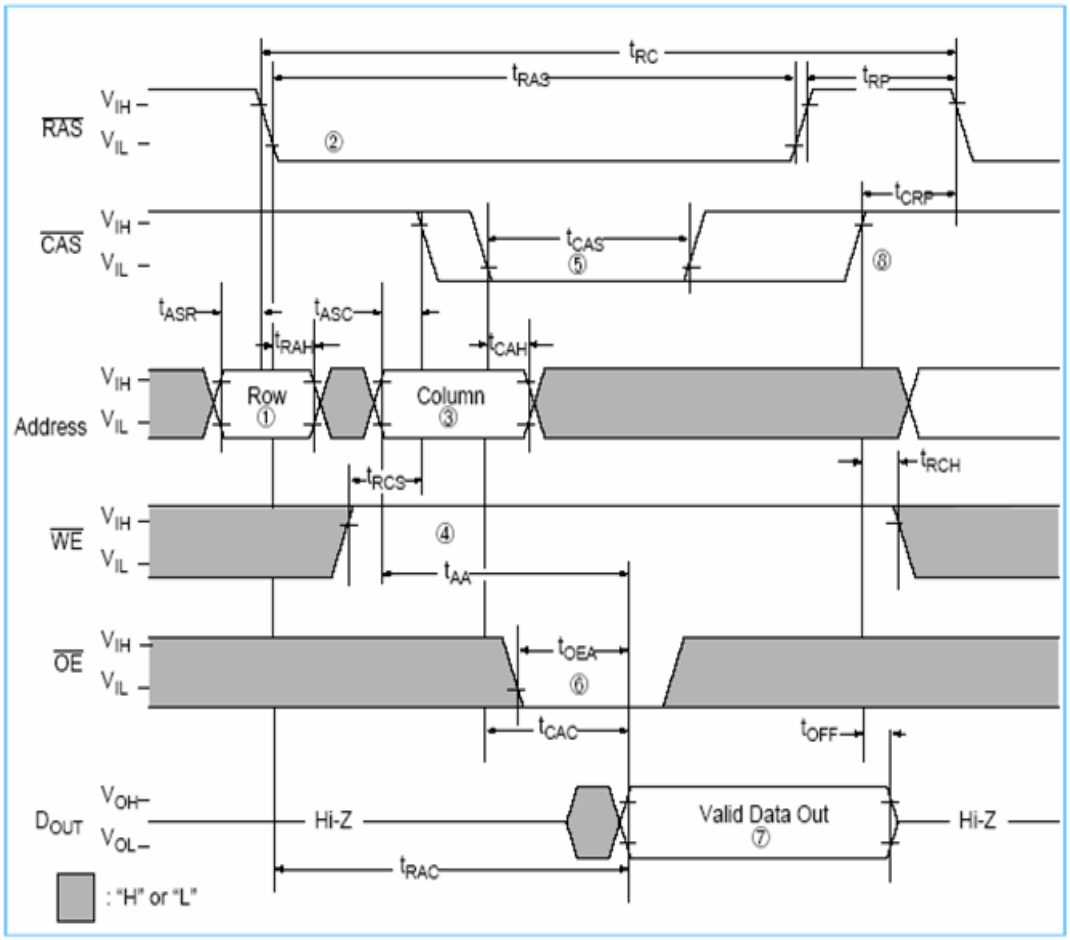
Reading Data From Memory

Figure 2 is the timing diagram of a simplified Read cycle that illustrates the following description.

To read the data from a memory cell, the cell must be selected by its row and column coordinates, the charge on the cell must be sensed, amplified, and sent to the support circuitry, and the data must be sent to the data output. In terms of timing, the following steps must occur:

1. The row address must be applied to the address input pins on the memory device for the prescribed amount of time before $\overline{RAS}$ goes low (t_{ASR}) and held (t_{RAH}) after $\overline{RAS}$ goes low.
2. $\overline{RAS}$ must go from high to low and remain low (t_{RAS}).
3. A column address must be applied to the address input pins on the memory device for the prescribed amount of time (t_{ASC}) and held (t_{CAH}) after $\overline{CAS}$ goes low.
4. $\overline{WE}$ must be set high for a read operation to occur prior (t_{RCS}) to the transition of $\overline{CAS}$, and remain high (t_{RCH}) after the transition of $\overline{CAS}$.
5. $\overline{CAS}$ must switch from high to low and remain low (t_{CAS}).
6. $\overline{OE}$ goes low within the prescribed window of time. Cycling $\overline{OE}$ is optional; it may be tied low, if desired.
7. Data appears at the data output pins of the memory device. The time at which the data appears depends on when $\overline{RAS}$ (t_{RAC}), $\overline{CAS}$ (t_{CAC}), and $\overline{OE}$ (t_{OEA}) went low, and when the address is supplied (t_{AA}).
8. Before the read cycle can be considered complete, $\overline{CAS}$ and $\overline{RAS}$ must return to their inactive states (t_{CRP}, t_{RP}).

Figure 2. Simplified Read Cycle



Writing Data To Memory

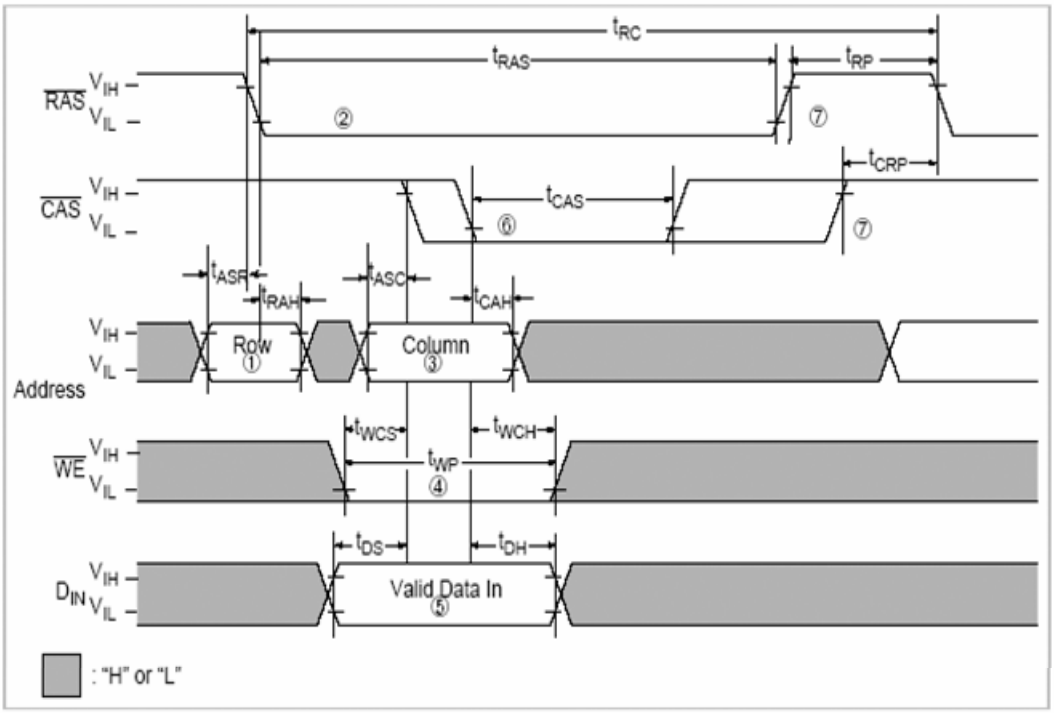
Figure 3 is the timing diagram of a simplified Write cycle that illustrates described below.

To write to a memory cell, the row and column address for the cell must be selected and data must be presented at the data input pins. The chip's on-board logic either charges the memory cell's capacitor or discharges it, depending on whether a 1 or 0 is to be stored. In terms of timing, the following steps must occur:

1. The row address must be applied to the address input pins on the memory device for the prescribed amount of time before $\overline{RAS}$ goes low and be held for a period of time.
2. $\overline{RAS}$ must go from high to low.
3. A column address must be applied to the address input pins on the memory device for the prescribed amount of time after $\overline{RAS}$ goes low and before $\overline{CAS}$ goes low and held for the prescribed time.
4. $\overline{WE}$ must be set low for a certain time for a write operation to occur (t_{WP}). The timing of the transitions are determined by $\overline{CAS}$ going low (t_{WCS}, t_{WCH}).
5. Data must be applied to the data input pins the prescribed amount of time before $\overline{CAS}$ goes low (t_{DS}) and held (t_{DH}).
6. $\overline{CAS}$ must switch from high to low.
7. Before the write cycle can be considered complete, $\overline{CAS}$ and $\overline{RAS}$ must return to their inactive states.

Note: There is considerable latitude within the memory chip's timings with respect to wOEhen data is actually written. The memory specifications show how to set up chip timings for early and delayed write options.

Simplified Write Cycle



Refreshing the Memory

Since DRAM memory cells are capacitors, the charge they contain can leak away over time. If the charge is lost, so is the data. To prevent this from happening, DRAMs must be refreshed -- that is, the charge on the individual memory cells must be restored periodically. The frequency with which refresh must occur depends on the silicon technology used to manufacture the memory chip and the design of the memory cell itself.

Reading or writing a memory cell has the effect of refreshing the selected cell. Unfortunately, not all cells are read or written within the time limitations. Thus each cell in the array must be accessed and restored during the refresh interval. In most cases, refresh cycles involve restoring the charge along an entire row. Over the course of the entire interval, every row is accessed and restored. At the end of the interval, the process begins again.

System designers have a lot of latitude in designing and implementing memory refresh. They may choose to fit refresh cycles between normal read and write cycles, or they may decide to run refresh cycles on a fixed schedule, forcing the system to queue read and write operations when they conflict with refresh requirements.

There are several different ways to refresh a memory array. The method you use will depend on the memory product you choose and the requirements of the system you are designing. Three common refresh options are briefly described below. Another refresh option is hidden refresh, in which a read or write operation and a refresh cycle are performed during a single $\overline{CAS}$ active period.

Using $\overline{RAS}$ Only Refresh (ROR)

Normally, DRAMs are refreshed one row at a time. The refresh cycles are distributed across the entire refresh interval in such a way that all rows are refreshed within the required interval. To refresh one row of the memory array using $\overline{RAS}$ Only Refresh, the following steps must occur.

1. The row address of the row to be refreshed must be applied at the address input pins.
2. $\overline{RAS}$ must switch from high to low. $\overline{CAS}$ must remain high.
3. At the end of the required amount of time, $\overline{RAS}$ must return high.

Using $\overline{CAS}$ before $\overline{RAS}$ Refresh (CBR)

To refresh one row of the memory array using $\overline{CAS}$ before $\overline{RAS}$ Refresh, the following steps must occur.

1. $\overline{CAS}$ must switch from high to low.
2. $\overline{WE}$ must switch to a high state (Read).
3. After the prescribed delay, $\overline{RAS}$ must switch from high to low.
4. An internal counter determines which row is to be refreshed.
5. After the required delay, $\overline{CAS}$ returns to a high level.
6. After the required delay, $\overline{RAS}$ returns to a high level.

The main difference between ROR and CBR is the method for keeping track of the row address to be refreshed. With ROR, the system must provide the row address to be refreshed. With CBR, the chip keeps track of the addresses using an internal counter.

Self Refresh (SR)

Self Refresh, also referred to as Sleep Mode or Auto Refresh, is unique because it uses an on-chip oscillator to determine the refresh frequency and a counter to keep track of addressing. SR is most often used for battery-powered mobile applications and applications that use a battery for backup power. While in sleep mode, the device uses extremely low current.

The timing required to initiate SR is a CBR cycle with $\overline{RAS}$ active for a minimum of 100 microseconds. The length of time that a device can be left in sleep mode is limited by the power source used. To exit, $\overline{RAS}$ and $\overline{CAS}$ are brought high.

Hardware Description

The MIO has 3 basic addressing areas: 1) ACIA at $D1C0-$D1DF, 2) MIO Latches at $D1E0-$D1FF, and 3) 256 bytes of RAM at $D600-$D6FF. Note that the ACIA and MIO latches are not fully decoded; both contain 4 read/write registers, but each register has 7 shadows. Tables 5-1 through 5-3 briefly describes the MIO registers.

ACIA Operation

For more information on the ACIA operation, refer to a 6551A or 65C51 data manual (this part is manufactured by Rockwell, GTE, NCR, and RCA). The only irregularity of usage is that the lines DSR, CTS, and DCD are tied to ground. This is due to the fact that the ACIA will not receive data if either of these lines are false. To read the actual state of these lines, you must read location $D1E3 (bits 2,1,0). This will return the true lines sense (DCD true is indicated by a high on bit 1 of $D1E3).

SASI/SCSI Interface

The data input/output ($D1E1) and input control lines ($D1E2) reflect the true voltage levels on the ports. Thus, the input control lines are normally all ones (port voltages are +5) which represents a logic false on the bus. For more information on SASI/SCSI bus protocol, refer to the Adaptec ACB-4000 Series User's Manual, the XEBEC S1410A disk controller document, the Seagate ST225N manual, or any other device manual employing these protocols.

The ACK-/REQ- handshake cycle is performed by the MIO hardware. Whenever the data ($D1E1) is read or written, ACK- is set true. It is cleared by a high level on the REQ- input signal.

The RST- is set true when $D1E0 is read or when the RESET key pressed on the computer (or during powerup). It is cleared by reading location $D1E2.

The I/O- controls whether the 8-bit printer/SASI registers are input or output. When I/O- is high (input to SASI controller), the data is output on the printer and SASI port. If I/O- is low, then the output latches are disabled (it will latch new data, but the output is tri-stated).

Printer Interface

The printer data ($D1E1) and BUSY signals are high true logic. The a high (1) on BUSY (bit 6 of $D1E2) indicates the printer is busy. A low (0) on FAULT- (bit 4 of $D1E2) reflects an error condition in the printer (printer off?).

Table 5-1. MIO Register Selection

Address (HEX)	Register Operation	
	Write	Read
$D1E0	Set address A15-A8 for $D600 RAM window. (LSB of sector number.)	Set RST- signal true (low). Resets the SCSI/SASI bus. (RST- also true during RESET)
$D1E1	Set printer data and SCSI/SASI data. True logic for printer — Inverted for SCSI/SASI bus.	Read data from SCSI/SASI bus. Data is inverted.
$D1E2	General purpose outputs. B[3..0] High RAM address, sets address A19-A16. B[4] 1 = Set SEL- true B[5] 1 = Enable RAM access B[6] 1 = Set STROBE- true B[7] 1 = Enable Parallel IRQ	General purpose inputs. B[0] = SASI C/D- B[1] = SASI MSG- B[2] = SASI I/O- B[4] = Printer FAULT- B[5] = SASI BUSY- B[6] = Printer BUSY B[7] = SASI REQ- Also clears RST- signal
$D1E3 or $D1FF	Set ROM enable and bank. Only 1 bit allowed set at a time. B[2] 1 = Disk Interface ROM B[3] 1 = Seg 2 of setup MENU B[4] 1 = R:/P: Handler ROM B[5] 1 = Seg 1 of setup MENU All bits 0 disable the ROM.	IRQ sense bits + Misc inputs. B[0] = RS-232 DCD line B[1] = RS-232 DSR line B[2] = RS-232 CTS line B[3] = Printer BUSY- IRQ B[4] = MIO IRQ (from 6551 or Printer BUSY- IRQ)
$D1C0	Write ACIA transmit register.	Read ACIA receive register.
$D1C1	Perform a programmed RESET on ACIA (data is "don't care").	Read Status register (resets IRQ). B[0] 1 = Parity error B[1] 1 = Framing error B[2] 1 = Overrun has occurred B[3] 1 = Receiver reg. full B[4] 1 = Transmitter empty B[7] 1 = IRQ occurred
$D1C2	Write ACIA command register. (see table 5-2)	Read ACIA command register. (see table 5-2)
$D1C3	Write ACIA control register. (see table 5-3)	Read ACIA control register. (see table 5-3)
$D6xx	Write RAM. High address A19-A8 selected by $D1E0/$D1E2.	Read RAM. High address A19-A8 selected by $D1E0/D1E2.

Table 5-2. ACIA Command Register

7	6	5	4	3	2	1	0
PMC							
PNC1	PNC0	PME	REM	TIC1	TIC0	IRD	DTR

Bits 7-6 **Parity Mode Control (PMC)**

7	6	
0	0	Odd parity transmitted/received.
0	1	Even parity transmitted/received.
1	0	Mark parity bit transmitted, parity check disabled.
1	1	Space parity bit transmitted, parity check disabled.

Bit 5 **Parity Mode Enable (PME)**

0 Parity mode disabled — no parity bit transmitted.
1 Parity mode enabled.

Bit 4 **Receiver Echo Mode (REM)**

0 Receiver normal mode.
1 Receiver echo mode — bits 2 and 3 must be zero for receiver echo mode, RTS will be true.

Bit 3-2 **Transmitter Interrupt Control (TIC)**

3	2	
0	0	RTS = false, transmitter disabled.
0	1	RTS = true, transmit interrupt enabled.
1	0	RTS = true, transmit interrupt disabled.
1	1	RTS = true, transmit interrupt disabled, and transmit break on TxD.

Bit 1 **Receiver Interrupt Request Disabled (IRD)**

0 IRQ- enabled (receiver)
1 IRQ- disabled (receiver)

Bit 0 **Data Terminal Ready (DTR)**

0 Data terminal not ready (DTR false)*.
1 Data terminal ready (DTR true).

Note
* The transmitter is disabled immediately. The receiver is disabled but will first complete receiving the byte in process.

Table 5-3. ACIA Control Register

7	6	5	4	3	2	1	0
	WL			SBR			
SBN	WL1	WL0	RCS	SBR3	SBR2	SBR1	SBR0

Bit 7 Stop Bit Number (SBN)

0 1 Stop bit.

1 2 Stop bits.

1 1/2 stop bits for WL=5 and no parity.

1 stop bit for WL=8 and parity.

Bits 6-5 Word Length (WL)

6	5	Number of bits
0	0	8
0	1	7
1	0	6
1	0	5

Bit 4 Receiver Clock Source (RCS)

0 External receiver clock (non-functional on MIO).

1 Baud Rate (SBR).

Bits 3-0 Selected Baud Rate (SBR)

3	2	1	0	Baud Rate
0	0	0	0	16 x RxC (Not usable by MIO).
0	0	0	1	50
0	0	1	0	75
0	0	1	1	110
0	1	0	0	135
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

Addressing the RAM

The MIO can access up to 1 Megabyte of RAM which takes 20 bits to address. Address bits A19-A16 are set from writing to the latch at $D1E2, bits A15-A8 are set from writing to the latch at $D1E0, and bits A7-A0 are CPU address lines A7-A0 when reading/writing $D6xx. Thus there are up to 4096 "pages" of memory that may appear at the $D6xx window.

In order to access the memory, it must first be enabled by setting $D1E2 bit 5 to "1" (this also turns on the MIO's red LED). It is generally a good idea to leave the RAM disabled while not using it in case of a system crash (which could inadvertently write in the $D6xx window).

When power is removed from the computer (for whatever reason), the MIO will continue refreshing its dynamic RAM. This is accomplished by its ability to maintain a 02 clock after the computers clock has stopped. VC1 adjusts the MIO's 02 clock frequency. Adjustment requires special equipment and should not be attempted.

Checking IRQ Status

The MIO has two sources of interrupts; one is the ACIA and the other is the parallel printer port. The printer port may interrupt the computer only if bit 7 of $D1E2 is set ('1') and the printer BUSY is false ('0'). Bit 4 of $D1E3 is the general IRQ flag from the MIO (a 1 indicates that IRQ- is true). If bit 3 is also set, then the IRQ- is caused by the printer. If not, then it must be the ACIA (in which case $D1C1 bit 7 should be set).

Note that the parallel device IRQ mask (PDIMSK at $249) is set to $10 by the MIO RAM. This is because, there is only one interrupt handler (which supports all possible MIO interrupts) in the ROM. In fact, the system would crash if the OS tried to enter any of the other ROM banks to service the IRQ.

Accessing the ROM

The ROM on the MIO contains all the software necessary to access the hard disk, the RAM, the ACIA (as an R: or P:), and the parallel printer port. It also contains the configuration which is downloaded into the computer RAM when SELECT+RESET are pressed.

The ROM is accessed as 4-2K banks. (An additional 8K is reserved for the 80 column adapter.) Bits 5-2 (of $D1E3) select which bank will be active (if any) at the $D800-$DFFF region. Only 1 bit may be set and its position selects which bank of ROM is active. If all bits are zero, then no banks are active and the Floating Point Math package in the OS ROM is enabled.

According to Atari spec, 1 device is to occupy one bank of ROM and that device has a specific address range legal to it at $D1xx. Since the MIO is an all inclusive device, however, it deviates from this spec. Instead, it tries to cram as much code as possible into a small space. This meant juggling the banks around to get along with the computer and to allow for expansion of an 80 column adapter. This is why there is only one interrupt handler, yet several input bits are returned in what is considered to be strictly an interrupt sense register (at $D1FF).

Software Description

In order for the MIO to perform its multitude of tasks, one full page of memory has been allocated for general operating variables and configuration parameters. Two other pages have been reserved for "R:" handler input and output buffers, and the rest of memory (up to 4093 pages) can be used as RAM drives and a printer buffer through the MIO ROM. Table 5-4 describes the configuration parameters (those which are read from the hard disk (ID=0, LUN=0) when memory is invalid). This table occupies the first 192 bytes of memory page 0. The remaining 64 bytes are operating variables and are listed in table 5-5. Memory pages 1 and 2 are reserved for the "R:" handler input/output buffers.

Table 5-4. MIO Configuration Parameters

Address (HEX)	Symbol Name	Length (Dec)	Function of parameter or variable.
$D600	MEMKEY	16	This contains a string of characters. If the string in memory is not equal to that in ROM, it is assumed that power to the MIO has been lost and it should reconfigure.
$D610	DRDATA	64	This contains an array of 8 drive config records (each 8 bytes long). Records are: +0: First physical block address (sector number) of logical device. MSB first. +3: Last+1 physical block address (sector number) of logical device. MSB first. +6: B[2,0] = SCSI/SASI ID if hard disk = drive number if floppy B[5] = 1 if floppy drive (reassign) B[6] = 1 if RAM drive B[7] = 1 if Hard drive if B[7,5] = 0, then ignore +7: B[3] = 1 if disk is write locked B[4] = 1 if SASI type interface B[7,5] = logical unit number of drive
$D652	PREND	2	Last+1 RAM page number allocated to print spooler.
$D654	PRUNIT	1	Printer device number (0 if P: disabled)
$D655	PRFLAGS	1	Printer configuration flags B[5] = 1 if using a serial printer B[6] = 1 if spooler is enabled B[7] = 1 if CR/LF option enabled
$D656	SERUNIT	1	RS-232 "R:" enable flag; 1=enable/0=disable
$D657	SERFLAGS	1	Default configuration for serial port. B[7] = 1 if to append LF after CR B[6] = 1 if 2 stop bits (else 1 stop bit) B[5] = 1 if no ATASCII/ASCII translation B[4,3] = parity mode: 00=none, 01=odd, 10=even, 11=mark B[2,0] = baud rate index
$D658	RAMUSAGL	8	Number pages allocated for each drive (low)
$D660	RAMUSAGH	8	Number pages allocated for each drive (hi)

$D668	RAMSIZE	1	Total number of RAM pages (high byte)
$D680	DRITYPE	64	Configuration data for SASI hard drives +0: Number cylinders on drive (MSB,LSB) +2: Numer heads on hard drive +3: Cylinder to start reduced write current +5: Precompensation value (usually 0) +7: ECC burst length (usually $0B)

Table 5-5. MIO Operating Variables

Address (HEX)	Symbol Name	Length (Dec)	Function of operating variable
$D6C1	CPRINPG	2	Printer queue character entry pointer. (memory page number) (LSB,MSB)
$D6C3	PRINPG	2	Printer queue character exit pointer. (memory page number) (LSB,MSB)
$D6C5	CPROFFS	1	Printer queue entry page offset.
$D6C6	PROFFS	1	Printer queue exit page offset.
$D6C7	BADBUFF	1	If 255, this indicates that the queue has wrapped, thus repeat copies are invalid.
$D6C8	PRIRQ	1	If 128, then parallel IRQ is enabled. This byte gets copied to $D6E2 when ROM exited.
$D6CA	PRPAUSE	1	If 0, then the printer spooler is paused.
$D6CB	PCOPYT	1	Number repeat copies to be printed (normally zero unless they get stacked)
$D6CC	SPOOLGO	1	Master spooler start/stop flag (255=go)
$D6CD	XON	1	XON/XOFF flag for serial printer handshake. 255=on 0=off.
$D6FC	CURPAGE	1	Shadow for $D6E0. Needed for IRQ operation.
$D6FD	SMISC	1	Shadow for $D6E2. Needed for IRQ operation.

RS-232 Handler Functions and Tables

This section contains a list of all input/output and XIO calls to the RS-232 "R:" handler of the MIO. Note that IOCB is an input/output channel number that indicates what OPEN device shall receive or provide data. For most XIO calls, you may use any legal IOCB number as long as it is NOT open to any other device. From Atari BASIC, you may use IOCB numbers 1 through 7 (0 is reserved for editing "E:" I/O).

Note that IOCB #7 is used for the BASIC LPRINT statement and IOCB #6 is used for graphics mode functions from BASIC. Also, if using SpartaDOS, IOCB #4 and IOCB #5 are used while doing output and input redirection respectively (via the DOS PRINT command and batch files).

All the syntaxes use just "R:" for the device name since there is only one RS-232 port on the MIO. In fact, if you do use a port number (ex. "R2:"), it is simply ignored and treated the same as "R:".

All the function formats are given in their Atari BASIC form. If using assembly language or some other high level language, refer to the language manual for its equivalent form.

Opening the RS-232 Port

Syntax
OPEN #IOCB,Aux1,0,"R:"

Remarks
This function opens a channel to the RS-232 port in pseudo "non-concurrent" mode. To remain compatible with the 850 and P:R: Connection, the MIO has a flag indicating whether an XIO 40 (set concurrent mode) has been performed since the last OPEN command. If it has not, then the STATUS command returns the state of the handshake lines, whereas if in concurrent mode, the STATUS command returns the number of characters in the input and output buffers.

Aux1 contains the I/O direction bits — 4 for input only, 8 for output only, and 12 for both input and output (which is equivalent to 13 of the 850 interface). Many XIO calls do not require that you open an RS-232 channel first, however, it is generally a good practice to open the channel first. Care should be taken when setting the state of the handshake lines; if you set DTR false, the transmitter and receiver are disabled. Therefore, you must re-enable them by setting DTR true before continuing with normal operation.

When the channel is opened, both the input and output buffers are cleared. Also, the RTS and DTR handshake lines are set true (to the ready state).

Closing the RS-232 Port

Syntax
CLOSE #IOCB

Remarks
This statement closes the IOCB connected to the RS-232 port. This simply shuts down the IOCB; the RS-232 port remains untouched except that the system waits until all data in the output buffer has been transmitted.

Input Character or Line From the RS-232 Port

Syntax
GET #IOCB,varb
INPUT #IOCB,varb$

Remarks
These functions input data from the RS-232 port; the GET statement inputs the numeric value of one character into a numeric variable and the INPUT statement inputs a string of characters into a string variable. On the INPUT statement, if the data is a numerical ASCII string, you may read the data into a numeric variable. Input strings are terminated by an end-of-line (EOL) character.

Note that the IOCB must be opened for read or read/write (modes 4 or 12), but whether in concurrent mode or not has no effect on GET/INPUT statement operation. Refer to your BASIC reference manual for more information on these statements.

Output Character or Line To the RS-232 Port

Syntax
PUT #IOCB,exp
PRINT #IOCB;exp$

Remarks
These functions output data to the RS-232 port; the PUT statement outputs the numeric value of one character to the port, and the PRINT statement outputs a string of characters to the port. The syntax of the PRINT statement is the same as a normal PRINT statement except that the "#IOCB;" precedes the expression.

Note that the IOCB must be opened for write or read/write (mode 8 or 12), but whether in concurrent mode or not has no effect on GET/INPUT statement operation. Refer to your BASIC reference manual for more information on these statements.

Reading the Port Status

Syntax
STATUS #IOCB,DUMMY
FLAGS = PEEK(746) : REM Error bits relating to status history
LINESTAT = PEEK(747) : REM Status of handshake lines
or
STATUS #IOCB,DUMMY
FLAGS = PEEK(746) : REM Error bits relating to status history
INCHARS = PEEK(747) : REM Number of chars in input buffer
OUTCHARS = PEEK(749) : REM Number of chars in output buffer

Remarks
These statement sequences are useful for determining many facts about the state of the RS-232 port. The first syntax is used when in pseudo "block mode I/O" (same as "non-concurrent"), whereas the second is used in concurrent mode I/O. Notice that the variable DUMMY is simply a CIO status of the success of the STATUS command. If there were an error (DUMMY<>1), then BASIC would halt and give an error message (unless a TRAP was performed prior to the STATUS).

The block mode STATUS (first syntax) returns a status history of the port (in FLAGS) and the state

of the control lines (in LINESTAT). The meaning of each bit is given in tables 6-1 and 6-2.

The concurrent mode STATUS (second syntax) returns a status history of the port (in FLAGS) and the number of characters in the input buffer (in INCHARS) and in the output buffer (in OUTCHARS). The meaning of each bit of FLAGS is given in table 6-1.

Table 6-1. Meaning of Error Bits From Location 746

Bit	Dec Equiv	Meaning of Error
7	128	Received a data framing error
6	64	Received a data byte overrun error
5	32	Received a data parity error
4	16	Received a buffer overflow error (>255 chars)

Table 6-2. Meaning of Status Bits From Location 747

Bit*	Dec Equiv	Meaning When Bit is Set (1)
7	128	DSR is true (ready)
5	32	CTS is true (ready — Always true on MIO)
3	8	CRX is true (ready)
0	1	RCV is at MARK (Always Set on MIO)

* Bits 6, 4, and 2 are simply copies of the next highest bit. In the 850 Interface, these bits would indicate a history (i.e. not always ready since last STATUS).

Forcing Early Transmission of Output Blocks

Syntax
XIO 32,#IOCB,0,0,"R:"

Remarks
This function causes all the buffered data in the computer to be transmitted through the RS-232 port. This is used when the user wants to make sure that all data is transmitted before performing his next function. (This could also be performed by doing status request until the output data length is zero.)

Controlling Outgoing Lines DTR, RTS, and XMT

Syntax
XIO 34,#IOCB,Aux1,0,"R:"

Remarks
This function allows you to set the state of the output handshaking lines. This function may be perform in both concurrent and "non-current" mode (there is really no difference except for the way STATUS commands are interpreted). Care should be taken when disabling DTR (setting to false) since transmission and receiving are halted until DTR is set TRUE. Aux1 is coded as indicated by table 4-3.

Table 6-3. Control Values Added to Aux1 (XIO 34)

Function	Bit	Dec Equiv	Meaning When Bit is SET
DTR	7	128	Set state of DTR (from bit 6)
	6	64	Set DTR Ready (Not ready if bit is CLEAR)
RTS	5	32	Set state of RTS (from bit 4)
	4	16	Set RTS Ready (Not ready if bit is CLEAR)
XMT	1	2	Set state of XMT (FROM BIT 0)
	0	1	Set XMT to MARK (SPACE if bit is CLEAR)

Setting Baud Rate, Stop Bits, and Ready Checking

Syntax
XIO 36,#IOCB,Aux1,0,"R:"

Remarks
This function configures the RS-232 port for desired speed and stop bits. Aux1 is the sum of two codes; baud rate and the number of stop bits. The coding is given by Table 6-4. You must add the value representing the desired baud rate to the code (0 or 128) for the desired number of stop bits per word. Note that the word size is always 8 bits plus 1 or 2 stop bits; the MIO "R:" handler does not support smaller word sizes as did the Atari 850 interface.

The "missing" baud rates are available through the ACIA on the MIO but are not supported by the "R:" handler since they are never used.

Table 6-4. Codes to Add to Aux1 (XIO 36)*

Add	Baud Rate	Add	Baud Rate
0	300	5	110
8	300	9	600
10	1200	12	2400
13	4800	14	9600
15	19200		

* Default is 1 stop bit. Add 128 for 2 stop bits.

Setting Translation Modes and Parity

Syntax
XIO 38,#IOCB,Aux1,0,"R:"

Remarks
This function configures the parity and level of ASCII/ATASCII translation. The value of Aux1 is derived from Table 6-5.

Table 6-5. Control Values Added to Aux1 (XIO 38)

Function	Add	Resulting Function Performed
PARITY	0	No parity (8-bit data is untouched) (default)
	4	Check/Set odd parity, clear parity bit
	8	Check/Set even parity, clear parity bit
	12	Send mark parity, clear parity bit
TRANS-	0	Light ATASCII/ASCII translation (default)
LATION	32	No translation
LINE	0	Do not append LF after CR (default)
FEEDS	64	Append LF after CR (translation from EOL)

Setting Concurrent Mode

Syntax
XIO 40,#IOCB,0,0,"R:"

Remarks
This function simulates the "Start concurrent mode I/O" of the P:R: Connection and Atari 850. This is needed because of the dual nature of the STATUS command. When in concurrent mode, the statement returns the size of the data buffers, whereas, when in "block mode", the statement returns the state of the handshake lines. This has no effect on the rest of the "R:" handler functioning or on the ACIA. It simply set a flag for the STATUS function.

Standard Printer & MODEM Cables

The following two tables are the standard connection specifications used for printer and MODEM cables. These should work for the most common printers and MODEMs or they may need to be modified according to the special needs of your particular installation.

Printer Cable Connections

36 pin centronics (male)		DB25P
1		1 - Data Strobe
2		2 - D0
3		3 - D1
4		4 - D2
5		5 - D3
6		6 - D4
7		7 - D5
8		8 - D6
16		18 – 25 - Gnd
32		15 - Fault
11		11 - Busy
9		9 - D7
Frame — to the shield wire	¶ ¶	No connection to shield

MODEM Cable Connections

DB25P		DB9P
20		4 - DTR
8		1 - CRX
2		3 - XMT
3		2 - RCV
7		5 - GND
6		6 - DSR
4		7 - RTS
5		8 - CTS
Frame — to the shield wire	¶ ¶	No connection to shield

The following table is used with a Toshiba P321 printer with serial interface and is only shown as a guide. All handshaking lines are connected even though most applications would work with only XMT, RCV, and GND. The Toshiba printer is a DTE device and the MIO is also a DTE device. This requires the crossing of XMT and RCV. Be sure to check your printer manual for pin out as most printer connectors will vary. If your serial printer is a DCE device (not DTE) then XMT would connect to XMT and RCV to RCV.

DTE Serial Printer Cable Connections

DB25P	DB9P
6 - DSR 4 - RTS	4 - DTR 1 - CRX
3 - RCV 2 - XMT	3 - XMT 2 - RCV
7 - GND 20 - DTR	5 - GND 6 - DSR
5,8 - CTS,CD 14 - FAULT	7 - RTS 8 - CTS
Frame — to the shield wire	No connection to shield

Null MODEM Cable Connections

This will allow transfer of files between an MIO serial port and an IBM PC or Atari ST without using MODEMs. Tie pins 6 and 8 together at the DB25 end (PC or ST).

DB25S	DB9P
8 - CRX 20 - DTR	4 - DTR 1 - CRX
3 - RCV 2 - XMT	3 - XMT 2 - RCV
7 - GND NC	5 - GND 6 - DSR
NC NC	7 - RTS 8 - CTS
Frame — to the shield wire	No connection to shield

Directly Compatable SCSI / SASI Devices

(as of firmware ver. 1.1)

Manufacturer	Model #	Interface	Drive type
Adaptec	ACB-4000A	SCSI	ST506/412
	ACB-4070	SCSI	ST506/412 (RLL certified)
Iomega	Alpha 10H	SCSI	(cartridge drive 10Mb)
	Beta xxx	SCSI	(cartridge drive xxMb)
Rodime	RO650	SCSI	(includes drive 10Mb)
	RO652	SCSI	(includes drive 20Mb)
Seagate	ST225N	SCSI	(includes drive 20Mb)
Western Digital	WD1002-SHD	SASI	ST506/412
XEBEC	1410	SASI	ST506/412
	1410A	SASI	ST506/412